UNIVERSITY OF OSLO
Department of Physics

Prototype Development of a Multi-Needle Langmuir Probe System

Master thesis

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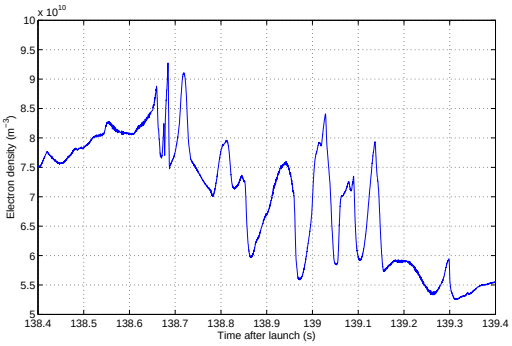

May 25, 2009

Abstract

This thesis deals with prototype development of a novel fixed-bias multi-Needle Langmuir Probe system (m-NLP). The system has been invented at UiO for use on sounding rockets and satellites. Measurement principles, instrument design, and calibration and test results are reviewed. In addition, the first results from the ICI-2 rocket campaign are presented.

The instrument works by measuring the current collected individually from four needle probes, placed in front of the rocket/satellite's shock front. The collected current is converted to voltage, filtered, digitalized and then sent to the central telemetry (TM) system for down link to the ground station. By using data from four fixed-bias Langmuir needle probes, sampled at the same time, the plasma electron density can be derived with high time resolution without the need to know the electron temperature and the spacecraft potential. With the selected needle probe design and the estimated electron densities, the instrument had to be capable of measuring currents down to 1 nA. Final performance of the electronics was a lower measurement limit of about 0.5 nA with satisfying signal-to-noise ratio. The maximum sample rate is about 9 kHz, but for the ICI-2 mission configuration a sample rate of 5787 Hz was used. This gives a spatial resolution of about 11 cm at payload apogee. Due to the configuration with four probes, the smallest physical structures that can be measured are limited by the probe distance of about 1 meter. With the selected probe size, the instrument can cover an electron density range from $n_e = 10^9 m^{-3}$ to $10^{12} m^{-3}$, and the four bias voltages for the probes can be set at any voltage between 0 V and 10 V.

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Tore André Bekkeng

Nomenclature

Abbreviations

Ammeter	Amperemeter
AA	Anti-Aliasing
ABT	Advanced Bi-CMOS (Bi-CMOS logic-family, combination of TTL and CMOS)
AC	Alternating Current
AGC	Automatic Gain Control
ADC	Analog to Digital Converter
bps	bits per second
CPLD	Complex Programmable Logic Device
CAD	Computer Assisted Design
DAC	Digital to Analog Converter
DAQ	Data acquisition
DC	Direct Current
FFI	Forsvarets Forskningsinstitutt
FPAA	Field-Programmable Analog Array
HF	High Frequency
FSM	Finite State Machine
IC	Integrated Circuit

ICI	Investigation of Cusp Irregularities
I/O	Input/output
IR	Infrared
JFET	Junction gate Field-Effect Transistor
JTAG	Joint Test Action Group
LAB	Logic Array Blocks
LE	Logical Element
LED	Light Emitting Diode
LF	Low Frequency
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCM	Pulse Code Modulated
rps	revolutions per second
Satcom	Satellite communication
SMD	Surface Mounted Devices
SOIC	Small-Outline Integrated Circuit
TM	Telemetry
TQFP	Thin Quad Flat Pack
VHDL	(VHSICHDL) Very High Speed Integrated Circuit Hardware Description Language

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Chapter 1

Introduction

This thesis describes the design, development and analysis of a novel fixed-bias multi-Needle Langmuir Probe System. The measurement principle was invented by PhD student Knut-Stanley Jacobsen at UiO. The system makes use of four needle probes biased with a different positive potential well above the platform potential, and a data acquisition (DAQ) unit. By using data from four Langmuir probes, sampled simultaneously, the electron density can be derived with high time resolution without the need to know the electron temperature and the spacecraft potential.

1.1 Background and Motivation

The motivation for this work was to make a Langmuir Probe instrument for the ICI-2 (Investigation of Cusp Irregularities) rocket payload. This sounding rocket was scheduled for launch from Spitsbergen in December 2008. The ICI-2 rocket flight would provide a first verification of UiO's multi-Needle Langmuir Probe concept. Inside the polar cusp, strong coherent HF backscatter echoes are found regularly. The relationship between the optical cusp and the HF radar cusp backscatter was first studied by Rodger et al. (1995) and in a number of papers since (e.g. Yeoman et al. (1997); Milan et al. (1997, 1998)). Moen et al. (2002) demonstrated that once HF backscatter was established, the optical cusp could be associated with a band of higher backscatter power and wide spectral widths. This was done by combining CUTLASS Finland radar observations above Svalbard with 2-D all sky camera images. The coherent HF radar can obtain backscatter echoes from plasma irregularities of decameter scale length.

In the northern regions the problem area is the auroral oval, and inside the entire polar cap, but the most important area of global interest is the

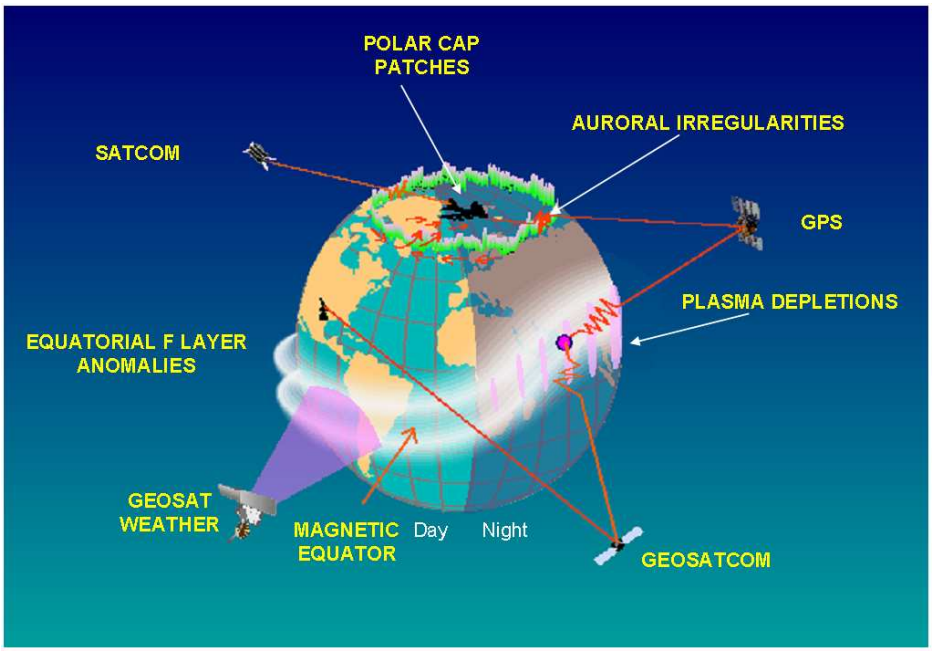


Figure 1.1: Global satellite communication outage regions.

equatorial region. Here the perturbations in the ionospheric plasma is caused by the force of gravity, instead of the force from the solar wind as in the polar regions. The global satellite communication (satcom) outage regions can be seen in Figure 1.1. In order to obtain a sufficient spatial resolution and a better understanding of ionospheric radio wave disturbances, in-situ measurements of the electron density in the space plasma have to be conducted. Langmuir probes are the best instrument for such measurements. To resolve the finest thinkable structures found in ionospheric plasma, limited by the electron gyro radius, a new high-speed sampling system was needed. Such a system can in a long perspective be of use in a global satellite network, mapping the structures and perturbations in the ionospheric plasma around the globe. This can result in a contribution to a space weather forecast for positioning and communication satellites. They suffer from scintillation (amplitude and phase distortion) of radio waves when the activity in the solar wind is high.

1.2 Goals of the Present Work

The main goal of this work was to develop a Langmuir probe instrument, capable of measuring current ranging from 1 nA to 1 μA, and with minimal noise. It also became important to make the probes as small as possible, as this affects the Debye shielding length for the probes. The Debye shielding length is the distance over which significant charge separation can occur, and this will affect how close the probes can be placed to each other. A second goal was to finish the instrument in time for the ICI-2 rocket campaign scheduled for launch in December 2008. The design started in January 2008, and the prototype had to be integrated at Andøya Rocket Range (ARR) in the beginning of June 2008. This gave about 5 months to build and test this prototype instrument. Laboratory testing at ESTEC and a successful ICI-2 rocket launch were the final goals, in order to give a proof of concept for the novel multi-Needle Langmuir Probe System.

Chapter 2

Langmuir Probes

Since the initial work of Mott-Smith and Langmuir (1926), Langmuir probes have been widely used to analyze plasma electron density and temperature; both in space and in the laboratory. The Langmuir probe works by placing an exposed conductor in a plasma, biasing it to a reference potential relative to the plasma potential, and measuring the collected current. There are two different types of probes; fixed bias and swept bias. The swept bias configuration has the advantage that it can determine both electron density n_e and electron temperature T_e. The long sweep time (up to 1 second) gives on the other hand a significant drawback in spatial resolution. The fixed bias configuration is used when high sample rates are needed, but it can not determine electron density or electron temperature. It can only give information about structures in the space plasma.

2.1 Probe-Plasma Coupling

When a probe is inserted into a plasma, it will acquire a floating potential, giving a net current to the probe equal to zero. In the high density plasma of the ionosphere the collected ambient electrons and positive ions will dominate the current balance. Since the mobility of electrons is significantly larger than the mobility of ions, the probe will acquire a negative potential. This will typically be a few volts with respect to the plasma potential. The reason for this is that the probe repels some of the electrons to equalize the currents. Because of the net charge of the probe, it will perturb the plasma in the immediate vicinity of the probe. This perturbed region is called the plasma sheath, and this shields the plasma outside the sheath from the electric field

of the body. The scale length of the sheath is given by the Debye length λ_D:

$$\lambda_D = \sqrt{\frac{\epsilon_0 k_B T_e}{n_e e^2}} \tag{2.1}$$

where n_e is the electron density, e is the electron charge, k_B is Boltzmann's constant, T_e is the electron temperature, and ϵ_0 is the permittivity of free space.

The probe size relative to the Debye length determines the sheath effects. The ideal case is when the probe scale size is significantly smaller than the Debye length. In that case sheath effects can be ignored. We assume a probe much smaller than the Debye length, measuring a Maxwellian plasma. For a spherical probe the current I_s due to collection of electrons is given by (Mott-Smith and Langmuir, 1926; Muralikrishna and Abdu, 1991):

$$I_s = n_e e \sqrt{\frac{k_B T_e}{2\pi m}} 4\pi r^2 \left(1 + \frac{eV}{k_B T_e}\right) \tag{2.2}$$

where m is the mass of an electron, r is the radius of the sphere and V is the potential of the probe relative to the ambient plasma.

The corresponding equation for a cylindrical probe, where the radius $r < \lambda_D$, is given by (Mott-Smith and Langmuir, 1926; Muralikrishna and Abdu, 1991):

$$I_c = n_e e \sqrt{\frac{k_B T_e}{2\pi m}} 2\pi r l \frac{2}{\sqrt{\pi}} \sqrt{1 + \frac{eV}{k_B T_e}} \tag{2.3}$$

where l is the length of the cylinder and I_c is the electron current for the cylindrical probe.

2.2 Current-Voltage Characteristics

A Langmuir Probe has an I/V characteristic that can be divided into three main regions.

A sufficiently negative biased probe will attract ions and repel electrons. The ion current will dominate, and this is called the "ion saturation region". When applying a sufficiently positive bias, the electron current will dominate. This is called the "electron saturation region". When the bias level is so high that the electron current dominates totally, the ratio between an increase in voltage and the probe current is linear. At an intermediate bias, neither the electron or the ion current will dominate. This is called the "retardation

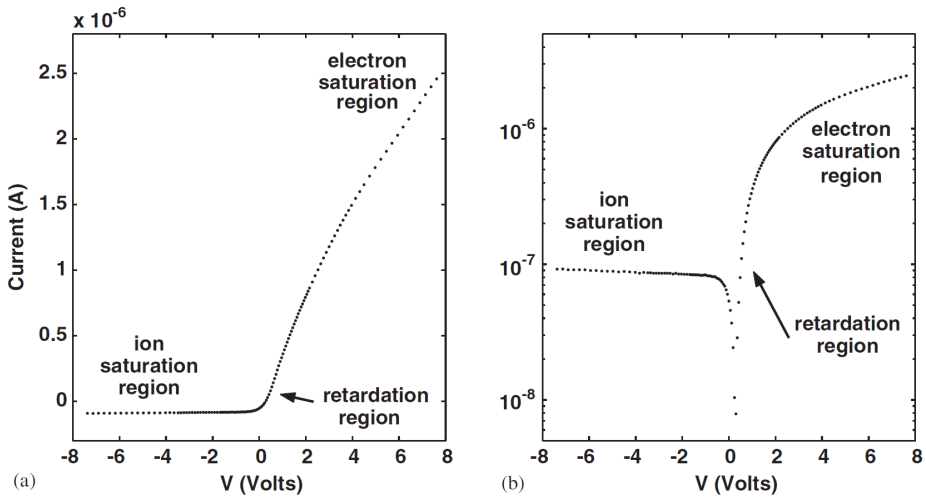


Figure 2.1: Langmuir Probe characteristics. Plot (a) has a linear current axis, and plot (b) has a logarithmic current axis.

region". With a single cylindrical or spherical Langmuir probe, the electron density n_e can be calculated from Eq.(2.3) or Eq.(2.2) respectively for the given values of I_c, T_e and V.

2.3 Measurement Principles

The two unknowns that we want to determine are the electron density n_e and the electron temperature T_e. However, the potential V is associated with a large uncertainty, since we do not know the spacecraft potential. The electron temperature is obtained by the slope of the retardation region in Figure 2.1, which is as straight line on a semi logarithmic scale:

$$T_e = \frac{e}{k_B A_{ret}} \tag{2.4}$$

where A_{ret} is the slope of the linear part of the I-V curve in Figure 2.1.

To get an I-V curve, the probe is swept from a negative to a positive voltage. The drawback of swept probes is that it takes time, in the order of 1 second, to complete one sweep that produces the current - voltage characteristic. There are also limitations on how fast the bias voltage can be swept while maintaining accurate measurements. As an operational concern,

a swept Langmuir probe voltage impress a signal on the plasma that often interferes with other experiments on the same platform (Pfaff et al., 1998). Sayers (1970) reviewed the in-situ probes available for ionospheric measurements, concluding that swept Langmuir probes will not give a better accuracy than $\pm$ 30% in electron density measurements. This is due to uncertainties in determining the spacecraft potential and the electron temperature, as well at sheath effects around the probe. Even though improvements in modeling the sheath effects have been done, the problems remain.

The other approach is the fixed bias probes. One probe at a fixed voltage gives just one point on the I-V curve in Figure 2.1. Although this type of probe can reveal structures in plasma it is impossible to determine the absolute value of the electron density with only one probe. The solution is to sample multiple probes simultaneously. This is reviewed in chapter 3.

Chapter 3

The Novel Langmuir Probe Concept

There was no established probe system available capable of measuring electron densities at meter scale resolution before the ICI-2 project. For the ICI-2 mission objective it was desirable to dissolve plasma structures of about 10 meters in size, with absolute measurements of n_e. This made high sampling rate a necessity. With a swept probe applying a 1 second sweep time, the spatial resolution for the ICI-2 rocket would be about 2.4 km. To achieve a high sampling rate and absolute measurements of n_e, the development of the m-NLP system was needed.

3.1 Langmuir Probe Theory for the Novel Probes

As the standard Langmuir probe technique of sweeping the bias cannot be performed rapidly enough, it was necessary to approach the problem by using a fixed bias. Since we are interested in the electron density, the probes have to be biased positively with reference to the plasma potential. The current measured is the sum of the electrons and the ions, so we have to be sure to be in the "electron saturation region". Here the ions are repelled and electrons are attracted. With a single Langmuir probe, the current can be calculated from Eq.(2.3) or Eq.(2.2). The two equations are almost the same, but Eq.(2.3) for the cylindrical probes makes it possible to take the square root of the term $(1+\frac{eV}{kT})$. The advantage from this fact is seen when Eq.(2.3) is squared.

$$I_c^2 = \frac{k_B T_e}{2\pi m}(nq2\pi rl)^2 \frac{4}{\pi}\left(1+\frac{qV}{k_B T_e}\right) = \frac{2k_B T_e}{m}(nq2rl)^2 + \frac{2q}{m}(nq2rl)^2 V \quad (3.1)$$

The first term is independent of V, and the second term is independent of T_e. Eq.(3.1) enables us to separate temperature from density. By using two probes with different bias, instead of one single probe, the equations for one probe can be subtracted from the other. The result is as follows:

$$I_{c2}^2 - I_{c1}^2 = \frac{2k_B T_e}{m}(n_e e 2rl)^2 - \frac{2k_B T_e}{m}(n_e e 2rl)^2 + \frac{2e}{m}(n_e e 2rl)^2 V_2 - \frac{2e}{m}(n_e e 2rl)^2 V_1 \tag{3.2}$$

$$\Delta(I_c^2) = \frac{2e}{m}(n_e e 2rl)^2 \Delta V \tag{3.3}$$

which is easily solved for n:

$$n_e^2 = \frac{m}{2e(e2rl)^2}\frac{\Delta(I_c^2)}{\Delta V} \tag{3.4}$$

$$n_e = \sqrt{K\frac{\Delta(I_c^2)}{\Delta V}} \tag{3.5}$$

where K is a constant equal to $\frac{m}{2q(q2rl)^2}$. The considerations for this result is discussed in section 3.1.1.

3.1.1 Probe Configuration

The novel Langmuir Probe concept is illustrated in Figure 3.1. If the bias on the probes is placed with good margin above the plasma potential, it is not necessary to know the probe potential relative to the plasma (V). Then the density is separated from temperature and spacecraft potential.

In an ideal world it would be sufficient with two probes, to determine the linear growth rate between I^2 vs V. In real life, abnormalities and noise will be hard to detect with only two probes. By using four probes it is be possible to get a good linear fit even with one defect probe. The defect probe can then be discarded for the linear fit, and this gives redundancy in case of probe defects. In order to reduce sheath effects it is desirable that the probes are as small as possible. However, a limitation is that a small probe collects less charge, and there is a limit to how small a current can be in order to be measured. For this measurement principle the information about the electron temperature T_e, which is an important parameter, has been sacrificed. However, measurements of T_e was not important for the ICI-2 mission.

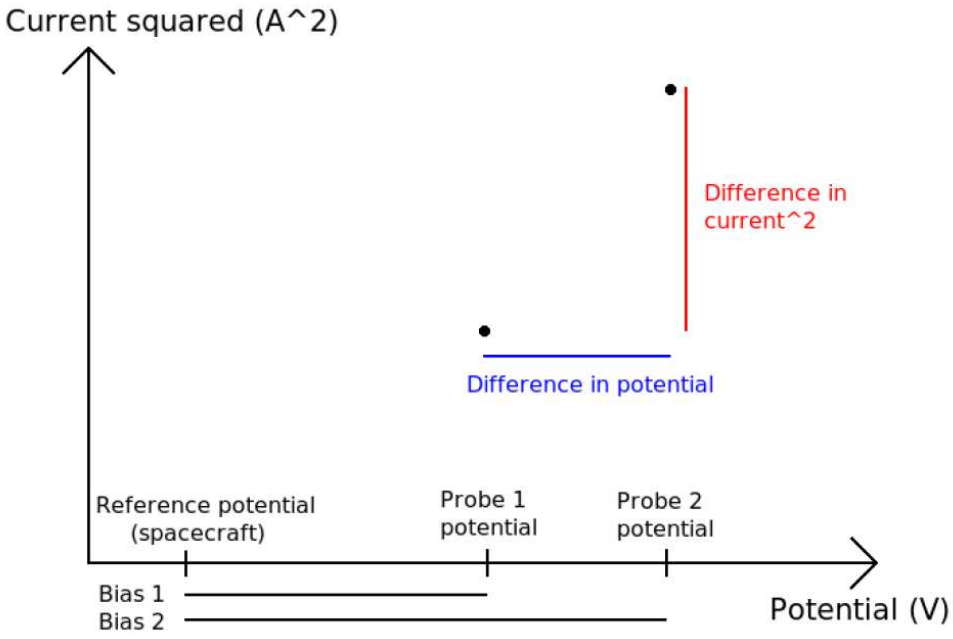


Figure 3.1: Two fixed bias cylindrical probes give us two points on a I^2 - V graph. The density is proportional to the square root of the slope of this graph.

Chapter 4

Principles of Current Measurements

When measuring low currents, a large number of error sources can influence the accuracy of the measurement. This section will describe the most common measurement circuits, as well as a description of noise sources. A noise analysis of the transimpedance amplifier in the m-NLP instrument is also included.

4.1 Current Measurement Circuits

In this section, two of the most common ammeter (amperemeter) circuits will be presented, showing advantages and disadvantages of the circuits. The most common source of error in any current measurement comes from the fact that the ammeter has a non-zero input resistance. This causes the current to be lower than before the meter was inserted in the circuit.

4.1.1 Shunt Ammeter

The shunt ammeter shown in Figure 4.1 works by inserting a resistance in the current path, and thus developing a voltage across this shunt resistor. The input current I_{IN} flows through the resistor R_{shunt}, giving the output voltage V_O:

$$V_O = I_{IN} R_{shunt}(1 + \frac{R_A}{R_B}) \tag{4.1}$$

For this ammeter circuit it is an advantage to use the lowest possible value for the resistor R_{shunt}. This gives better accuracy, as well as temperature and

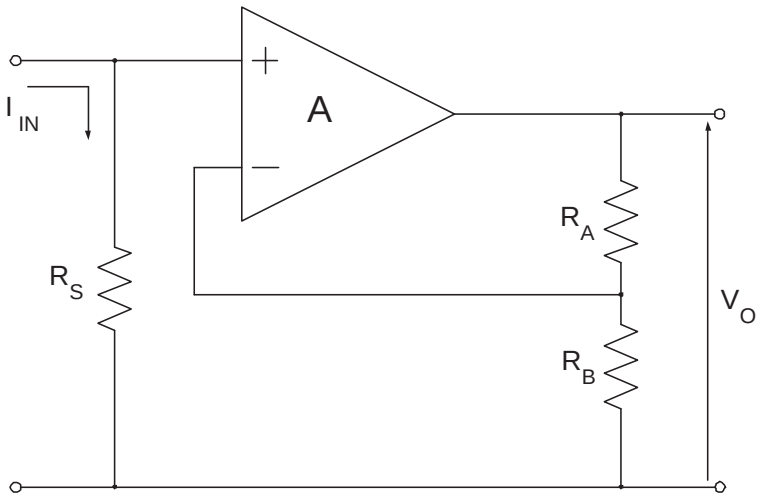


Figure 4.1: Shunt ammeter

time stability, giving faster response time. The disadvantage of choosing a small resistor (R_{shunt}) is that the signal-to-noise ratio will be decreased. This happens due to a low voltage drop over the resistor when R_{shunt} is low. The main problem with the shunt ammeter is the inherently high input resistance. In order to measure a very low current the shunt resistor R_{shunt} must be very large to generate a sufficient voltage across R_{shunt}. However, a large shunt resistance reduces the current to be measured.

4.1.2 Feedback Ammeter (Transimpedance Amplifier)

The feedback ammeter, also referred to as a transimpedance amplifier, is shown in Figure 4.2. It works by current I_{IN} flowing through a feedback resistor R_F. This gives the following output voltage V_O:

$$V_O = -I_{IN} R_F \tag{4.2}$$

The feedback ammeter is the best circuit for measuring low currents, since it does not cause the measured current to decrease when using a large feedback resistor R_f. The sensitivity of the ammeter is determined by the feedback resistor R_F. When connecting a feedback resistor to an operational amplifier (op-amp), it will become stable for high gains. For low gains, normally for gains equal to 5 and below, many op-amps will begin to oscillate when connecting a feedback resistor. To avoid this a feedback capacitor can be

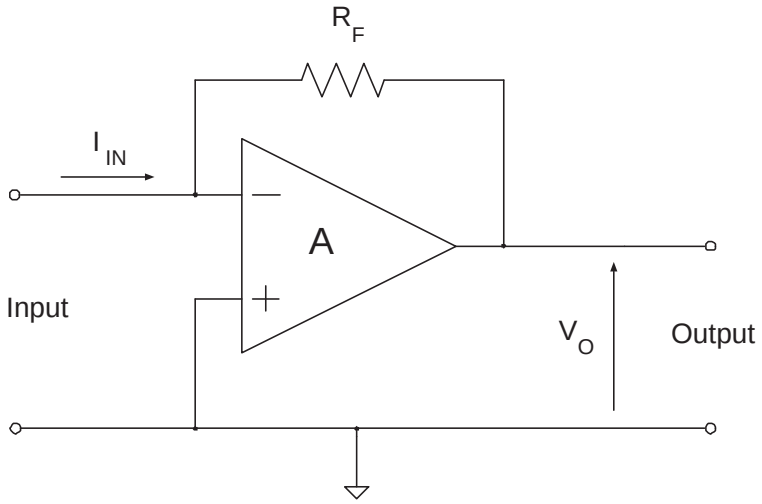


Figure 4.2: Feedback Ammeter

added across R_F to stabilize the amplification circuit.

Figure 4.3 shows the equivalent circuit for an op-amp input stage, equivalent to the notification described by Fraden (2003). e_o is the input offset voltage, e_n is the input noise voltage, i_o is the input offset current and i_n is the input noise current. R_S and C_S represents the sensor's resistance and capacitance, R_L and C_L represents the op-amp's load resistance and load capacitance.

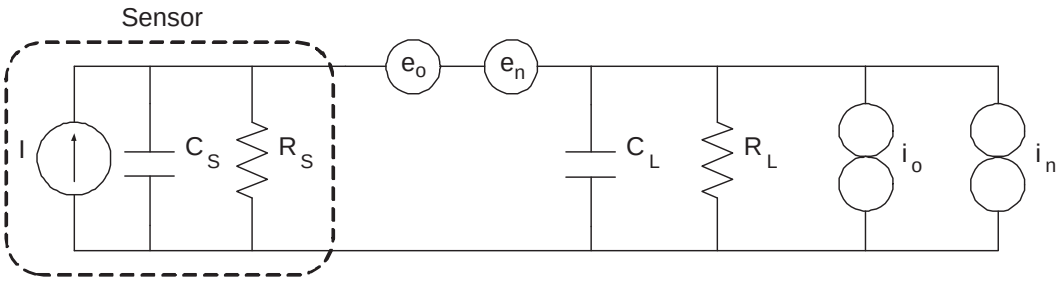


Figure 4.3: Amplifier equivalent circuit with current and voltage error sources

i_o and e_o are deterministic error sources, and can be subtracted from the output based on calibration. However, it is desirable to choose an amplifier with low i_o and e_o. i_n and e_n are stochastic (random) error sources that cannot be compensated by performing a calibration.

From Figure 4.3 the following specifications is of great importance for low noise performance:

- Low input voltage noise density ($nV/\sqrt{Hz}$)
- Low input current noise density ($pA/\sqrt{Hz}$)
- Low input capacitance

The two first specifications are vital to the signal-to-noise ratio. For stability a low input capacitance is of most importance. The feedback ammeter is the best ammeter circuit when measuring low currents. Choosing a small feedback resistor will result in a low gain, and therefore a low signal-to-noise ratio for low currents. However, a large feedback resistor will result in a slow response.

4.2 Noise Sources

When designing analog circuits, several sources of noise has to be taken into consideration. This section will look into three of the most common noise sources.

4.2.1 Thermal noise

Thermal noise is also called Johnson noise or Nyquist noise. Its source is thermal motion of charge carriers in a resistive element. The electrons flowing through the resistor will get a random component to their motion, and the random motion increases with temperature. At absolute zero, thermal noise will be absent. The power density of thermal noise is constant over all frequencies (white noise), and independent of current flow.

Below 100 MHz, Nyquist's relation can be used to calculate the thermal noise E_{th} in rms voltage (TI, 2000):

$$E_{th} = \sqrt{4k_B T R \Delta f} \tag{4.3}$$

This gives the following expression for the thermal current noise:

$$I_{th} = \sqrt{\frac{4k_B T \Delta f}{R}} \tag{4.4}$$

where I_{th} is the thermal noise current (in A rms), k_B is Boltzmann's constant, T is temperature in K, R is resistance and Δf is the noise bandwidth in Hz.

4.2.2 Shot Noise

Shot noise is associated with dc current flowing across a potential barrier, such as an pn junction. The random arrival rate of charge carriers crossing the potential barrier creates a fluctuating current, called shot noise. This noise is independent of temperature and stops when the current flow stops, and it has a flat power density (white noise).

The rms shot noise current is equal to (TI, 2000; Sarpeshkar et al., 1993):

$$I_{sh} = \sqrt{2eI_{dc}\Delta f} \tag{4.5}$$

where e is the electron charge ($1.6 \cdot 10^{-19}$ coulomb), I_{dc} is the average forward dc current and Δf is the noise bandwidth in Hz.

4.2.3 1/f noise (Flicker noise)

Flicker noise is a strong function of frequency, and most important at low audio frequencies. It has the following characteristics (TI, 2000):

- It increases as the frequency decreases, hence the name 1/f
- It is associated with a dc current in electronic devices
- It has the same power content in each octave or decade

According to TI (2000) the current noise I_f is given as:

$$I_f = K_i \sqrt{(ln\frac{f_{max}}{f_{min}})} \tag{4.6}$$

where K_i is a proportionality constant representing I_f at 1 Hz, and f_{max} and f_{min} are the minimum and maximum frequencies in Hz. The causes of the flicker noise are not completely understood. The frequency at which the shot noise equals the flicker noise is called the flicker-noise corner frequency.

4.3 Noise analysis of the transimpedance amplifier

The noise sources of the transimpedance amplifier is shown in Figure 4.4:

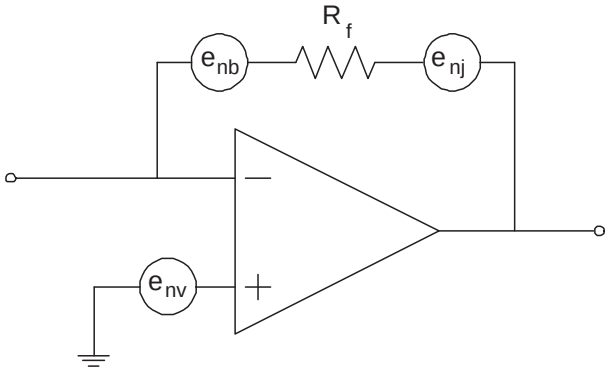


Figure 4.4: Noise equivalent circuit for the transimpedance amplifier

where e_{nb} is the input current noise multiplied by the feedback resistance R_f, e_{nv} is the input voltage noise and e_{nj} is thermal noise (Johnson noise).

The input voltage noise e_{nv} is always represented by a voltage source in series with the non-inverting input. For the lowest noise, resistor values should be kept as small as possible. However, in a transimpedance amplifier the feedback resistor R_f is the only resistor. This resistor is usually large to get a high gain. For a low R_f the op-amp voltage noise e_{nv} dominates. For very high R_f the input current noise e_{nb} dominates. This causes the $e_{nb} = I_n \cdot R_f$ in Figure 4.4 to be the dominating voltage source. The voltage noise sources are assumed to be independent (not correlated), and the total noise in the system is

$$e_{tot} = \sqrt{e_{nv}^2 + e_{nj}^2 + e_{nb}^2} \tag{4.7}$$

In order to get some numbers for the different noise sources the LT1793 operational amplifier is selected as an example. This is a high performance op-amp, with the following specifications:

- Input noise current density: 0.8 fA/$\sqrt{Hz}$
- Input noise voltage density: 8 nV/$\sqrt{Hz}$

Assuming a feedback resistance of 5 MΩ, a bandwidth of 3 kHz and room temperature (20^oC or 293.1 K) gives:

$$
\begin{aligned}
e_{nb} &= 0.8 \text{ fA}/\sqrt{Hz} \cdot 3 \text{ kHz} \cdot 5 \text{ M}\Omega = 0.22 \ \mu V \\
e_{nv} &= 8 \text{ nV}/\sqrt{Hz} \cdot 3 \text{ kHz} = 0.44 \ \mu V \\
e_{nj} &= \sqrt{4k_B T R \Delta f} = \sqrt{4 \cdot k_B \cdot 293.1 \text{ K} \cdot 5 \text{ M}\Omega \cdot 3 \text{ kHz}} = 15.6 \ \mu V \\
e_{tot} &= \sqrt{e_{nv}^2 + e_{nj}^2 + e_{nb}^2} = \sqrt{(0.44 \ \mu V)^2 + (0.22 \ \mu V)^2 + (15.6 \ \mu V)^2} \\
&= 15.6 \ \mu V
\end{aligned}
$$

The transimpedance amplifier's signal-to-noise ratio (S/N) in dB is given by:

$$S/N(dB) = 20 \ log_{10}[\frac{I \cdot R_f}{e_{tot}}] \tag{4.8}$$

Assuming that S/N = 1 is the threshold for detectability. This corresponds to S/N(dB) = 0, which gives:

$$log_{10} \frac{I \cdot R_f}{e_{tot}} = 0 \tag{4.9}$$

This gives

$$I = \frac{e_{tot}}{R_f} \tag{4.10}$$

Assuming $e_{tot} = 15.6 \ \mu V$ and $R_f = 5 \ M\Omega$ gives that the lowest detectable current is about 3 pA. However, S/N ratio of 1 is usually not sufficient: In order to have a good detectability it would be favorable to have a S/N ratio of about 10.

Chapter 5

Design of the m-NLP instrument

This chapter will look into the requirements for the m-NLP instrument, and give a review of the mechanical and the electrical design.

5.1 General requirements

The electron densities to be measured by the ICI-2 rocket payload was estimated to be in the range of $n_e = 10^9\ m^{-3} - 10^{12}\ m^{-3}$. The corresponding currents to be measured by the instrument, given these densities and the selected probe dimensions, was calculated to be in the order of 1 nA to 1 μA. The space available for the m-NLP instrument box on board the ICI-2 payload was $105 \cdot 85 \cdot 65\ mm^3$. The preferred location for the instrument box was on the top-deck. This gave less space than if the instrument had been located in the instrument section of the payload. The requirements for the probe size is described in section 3.1.1. The mounting of the probes had to be done in such a way that the probes were electrically isolated from the rocket. The reason for this is that the rocket acquires a floating potential that is different from the fixed probe biases.

In addition there were other operational requirements for the instrument:

- Withstand heavy vibrations during launch.
- Operate in temperatures up to 70 ^oC, and withstand relatively fast temperature changes. (Based on measurements onboard previous sounding rockets the temperature on the top deck was not expected to get higher than 70 ^oC).
- Power consumption below about 150 mA at 28 V supply voltage.
- Probe diameter several times smaller than λ_D.

5.2 Mechanical Design

This section describes the mechanical design of the electronics box and the E-field boom system which the Langmuir probes are mounted on.

5.2.1 Electronics box

The dimensions of the box was selected to be $100 \cdot 75 \cdot 50\ mm^3$ in order to fit inside the available space onboard the ICI-2 payload. The design of the box was done by Jan Kenneth Bekkeng, using SolidWorks, and then produced at the mechanical workshop at UiO. The box is made of five parts: The box itself, the upper lid, a shielding lid around the connectors and two L-shaped brackets for mounting to the payload top deck. The lid and mounting brackets have a thickness of 2 mm, and the rest box is 2 mm thick in all flat surfaces. In the rounded corners the box is up to 4 mm thick.

A design with a mountable lid on top was chosen for easy insertion and inspection of the electronics. The shielding lid was added to the box later on. This was done to protect the electronics from possible debris coming from the nose cone separation and boom deployment, as well as for protection during testing. The box could have been made smaller; it contains only two circuit boards but has space for three. The 3D computer assisted design (CAD) of the box can be seen in Figure 5.1.

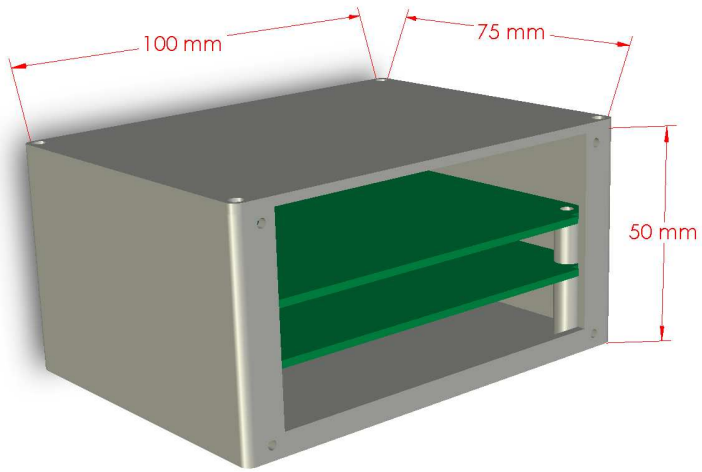


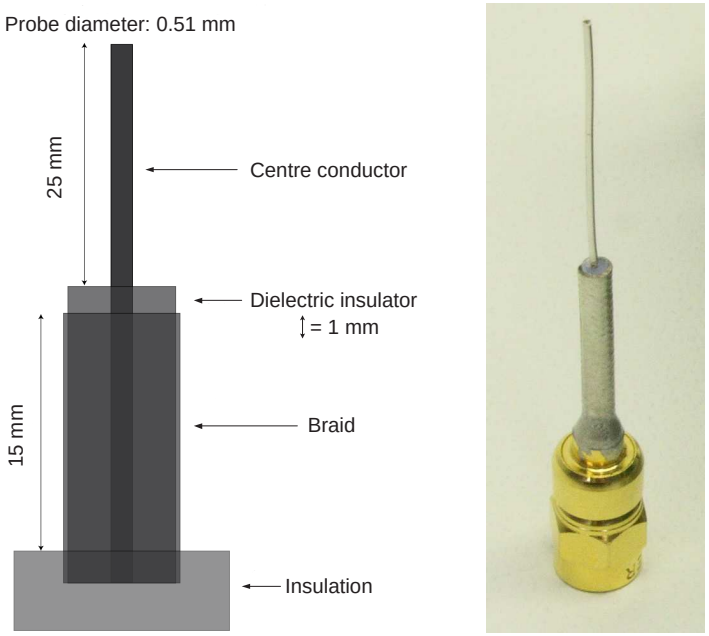
Figure 5.1: Electronics box dimensions

5.2.2 Needle probes

The needle probes needed to have a very small diameter (about 0.5 mm), and have a sufficient mechanical strength to withstand heavy vibrations during launch. In order to reduce sheath effects, it is desirable to have the probes as small as possible, about 1/10 of the Debye shielding length. For prototyping the probes several semirigid coax cables were tested. The prototypes were made by using a scalpel to strip the coax cable, according to Figure 5.2. The center conductor of the coax cable, with a length of 25 mm, works as the cylindrical probe. The insulation on the remaining 15 mm of the braid was removed as well, in order to avoid charging of insulation material close to the probe. A very short insulation area was kept after the braid, in order to avoid a short-circuit between the braid and the center conductor. Other solutions were considered, but these made it inconvenient to get a good method for mechanical mounting and electrical contact. The solution with the semirigid coax cable was therefore chosen for its advantages for in-house production and short production time. The final decision was to use the Habia Flexiform 405 FJ. The specifications and the mechanical properties for the finalized probe is found in table 5.1. These specifications are based on the simulation results made by PhD student Knut Stanley Jacobsen.

Parameter	**Specification**
Overall length	40 mm
Braid length	15 mm
Probe length	25 mm
Probe diameter	0.51 mm
Impedance	50 Ω
Center conductor	silver-plated copper-clad steel wire
Dielectric	solid extruded polytetrafluoroethylene (PTFE)
Braid / shield	tin-soaked copper braid, 100% coverage
Maximum bias voltage	$\sim 1500V$
Connector	Suhner SMC

Table 5.1: Needle probe specifications



(a) Technical probe drawing

(b) Manufactured probe

Figure 5.2: The m-NLP instrument probe

5.2.3 Boom Deployment System

In front of the payload the four needle probes are mounted on the E-field boom deployment system. The placement is about halfway out from the center of the structure, see Figure 5.3. This gives a probe separation of about 97 cm when the booms are fully extended.

Each probe is mounted using a RG 178 SMC connector, which is mounted to the boom structure on a piece of isolating material; see Figure 5.4. During launch the booms are folded together in the rockets longitudinal direction. When the booms deploy they fold out radially from the rocket by the centrifugal force created by the rocket spin. From each probe a RG178 coaxial cable runs inside the boom structure, down to the DAQ unit mounted on the top deck.

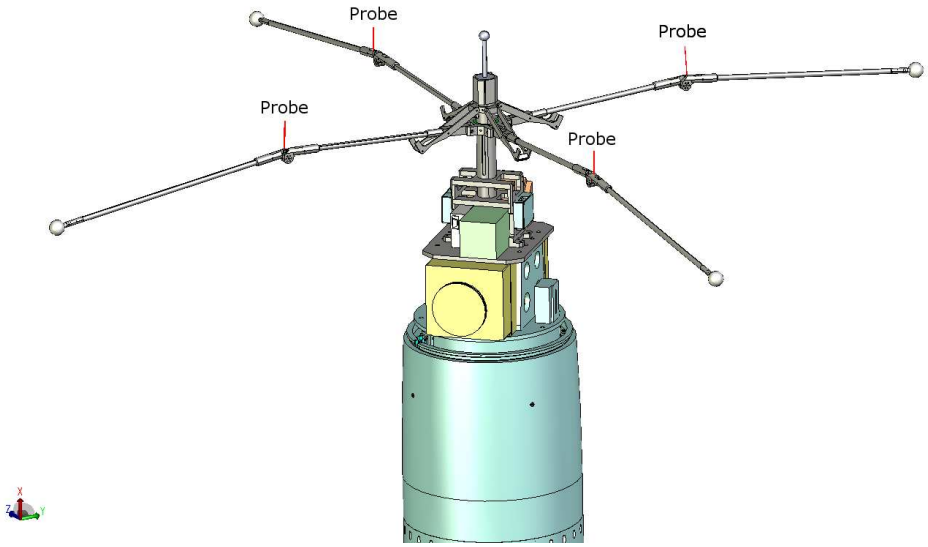


Figure 5.3: Boom geometry

Figure 5.4: Probe placement on boom

5.3 Electrical design

The m-NLP instrument contains two four-layer PCBs; one data acquisition card (DAQ) and one power/interface card. The DAQ card's front-end has four current measurement channels, with current-to-voltage converters, differential amplifiers, passive RC-filters and programmable 8th order elliptic anti-aliasing filters. The analog signals are digitalized in a 16 bits analog-to-digital converter (ADC). A Complex Programmable Logic Device (CPLD) contains all the digital control logics of the instrument. The power/interface card performs voltage regulation and contains the communication interface to the rocket encoder. The two PCBs are connected together with card-to-card connectors made of two gold plated pinrows and mating connectors, giving a spacing of about 10 mm between the PCBs. Components are mainly surface mounted devices (SMD). They are smaller than hole mounted components and could contribute to lower noise a high frequencies.

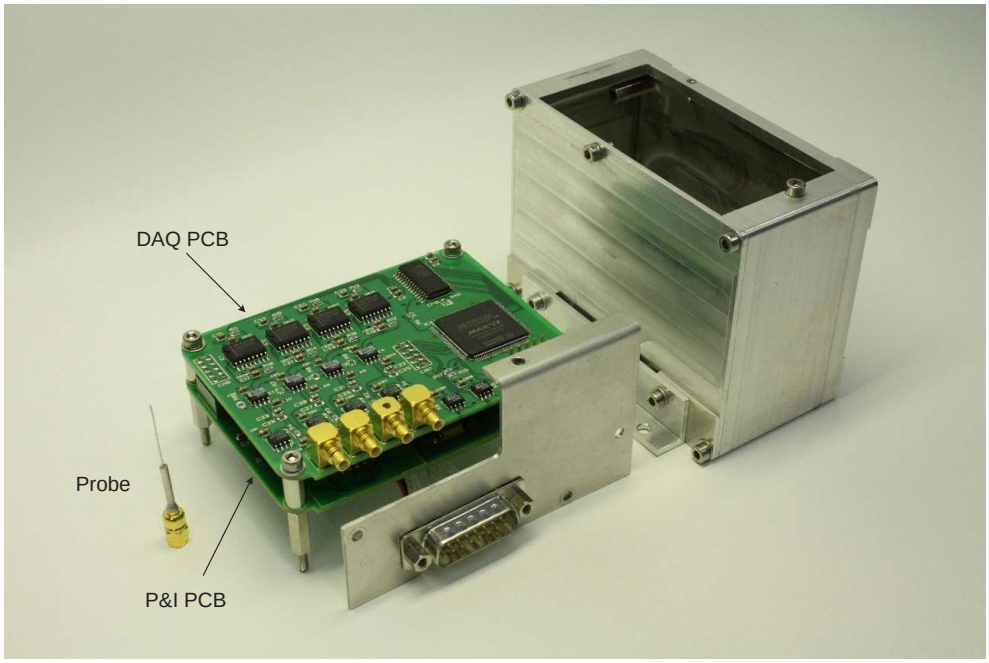


Figure 5.5: The m-NLP instrument

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Figure 5.5 shows the components in the m-NLP instrument. It contains of four needle probes (only on is shown here), two PCBs that are connected by two pinrows and mating connectors, and an electronics box made of aluminium. The boards are mounted together and inside the box using distance

spacers and machine shrews.

5.3.1 Power and Interface PCB

This circuit board handles voltage regulation and the interface against the rocket encoder. It has a mix of SMD and hole mounted components. All components are mounted on the top-side of the board, and schematics and PCB layout for the board is found in appendix A.2.

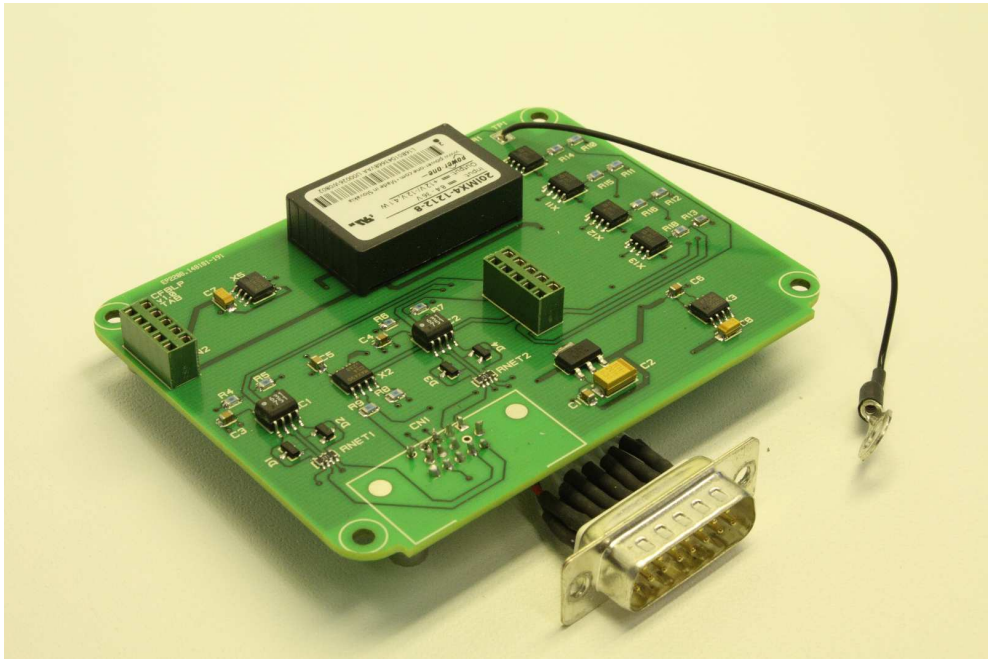

Figure 5.6: Power and Interface PCB.

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Overview of the Telemetry Interface

The rocket encoder has the following signals to and from the instrument:

SCLK System clock from encoder. (3.33 MHz used for ICI-2), 50% duty-cycle

GATE Data control signal from encoder. Active high when data transmission from the instrument

MINF Minor Frame. Synchronization signal from the encoder. Synchronize the instrument against the encoder framerate (2 893,5 frames/s for ICI-2)

MAJF Major Frame. Synchronization signal from the encoder. Synchronize the instrument against the encoder framerate (45,21 formats/s for ICI-2)

DATA Digital line for serial data transmission from the instrument to the rocket encoder

The signals SCLK, GATE, MINF and DATA are used for communication with the PCM encoder. GATE goes from low to high on the falling edge of SLCK. At the first rising edge on SCLK after GATE goes high from the encoder, MSB must be made available on the DATA line. MSB will then be read by the encoder about when the next falling edge on SCLK occurs. MSB-1 is made available on the data line when SCLK again goes high. This repeats until finally LSB is made available on the DATA line, on the first rising edge of SLCK after GATE has gone low again; see Figure 5.8.

Interface Electronics

Figure 5.7 shows the pulse code modulated (PCM) interface schematics. Optocouplers are used to get a galvanic isolation between the instrument and the rocket encoder. This will make the instrument capable of handling several volts in difference between the ground planes on the instrument and the encoder. It will also break any ground loops. The optocouplers chosen for the interface is HP0631 from HP. These have open-collector output, and therefore need a pull-up resistor. The optocoupler output is pulled up to 3.3 V. This is the maximum accepted voltage in on the CLPD without a resistor in series with the input signal. From experiences made by Bekkeng (2002) the input and return lines on the HP0631 should have a 220 Ω resistor, in order to get a total resistance that give sufficient current through the optocoupler diode, within the operational range of the optocoupler. A signal diode is placed on the optocoupler inputs, as this will protect the optocoupler if wrong connections are made. The optocoupler inverts the signal, and therefore the signal is inverted once again in the CPLD for correct data timing. For data transfer a MAX490 RS422 circuit is chosen. No external components are necessary, except from bypass capacitors.

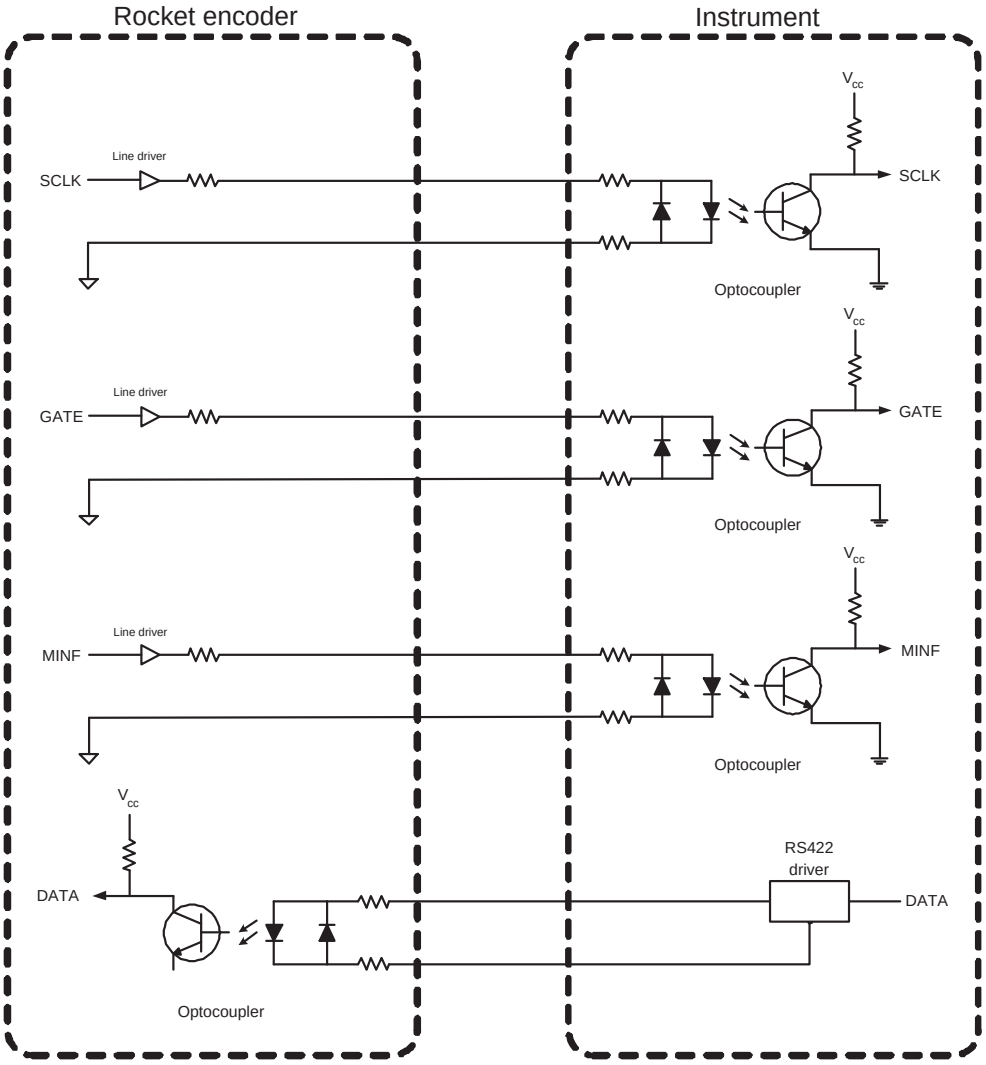

Figure 5.7: Electronics interface between the instrument and the rocket encoder

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Voltage Regulation Electronics

The input power accepted by the instrument ranges from 8.4 V to 36 V. This design requires five voltages for the integrated circuits: +3.3 V, +5 V, -5 V, +12 V and -12V. In addition, four bias voltages is needed for probe biasing: +2.5 V, +4.0 V, +5.5 V and +7.0 V. Only 28 V is available from the power distribution system in the rocket. For ±12 V a DC-DC switched regulator

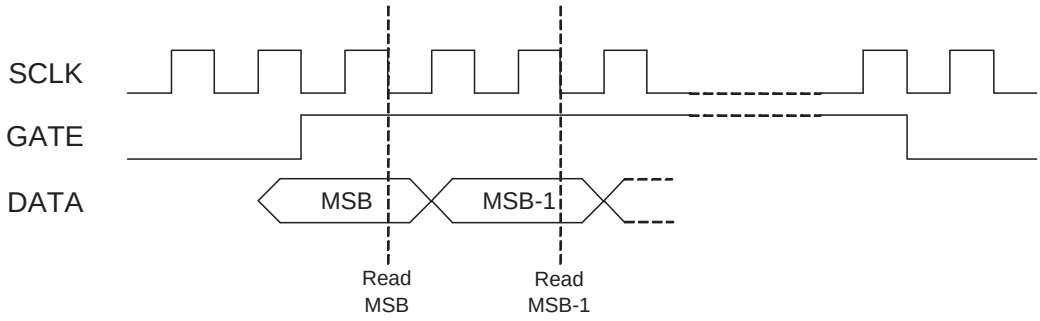

Figure 5.8: Timing diagram for PCM data transfer

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is used. Linear regulators are use behind the switched supply for ±5 V and +3.3 V output generation. Linear regulators have a much smaller efficiency than switched regulators. However, the backdraft of switched regulators is that they produce a small ripple on the output. The entire instrument will use about 3.5 watt (measured in lab) at 3.33 MHz clock frequency. The main contribution to this is the digital programmable filters, which use 762 mW each. A switched regulator from Power-one (20IMX4-1212-8), capable of delivering 4.1 W, is used due to the actual demands for input voltage. It gives ±12 V, and 0.35 A at both the positive and the negative output. The accepted input voltage ranges from 8.4 V to 36 V (Power-one, 2006). The maximum output ripple is 120 mV; no external components are needed after this regulator. For lower output ripple, a 4.7 μF ceramic capacitor is recommended close to the output.

To get the voltage down to +5 V a 78L05ACM linear regulator is used. A 100 nF ceramic capacitor is used between input and ground, and a 1 μF tantal capacitor is used between output and ground. To get the voltage down to -5 V a 79L05ACM linear regulator is used. Again a 100 nF ceramic capacitor is used between input and ground. A 1 μF tantal capacitor is used between output and ground. Both 78L05ACM and 79L05ACM is in 8 pin SOIC (Small-outline Integrated Circuit) packages.

To get the voltage down to +3.3 V another linear regulator (LM1117MP) is used. A 100 nF ceramic capacitor is used between input and ground, and a 10 μF tantal capacitor is used between output and ground. The four different bias voltages for the probes are produced using a 10 V voltage reference (AD587) and a voltage divider (using two resistors) for each of the bias voltages, followed by a unity gain amplifier for buffering.

5.3.2 Data Acquisition PCB

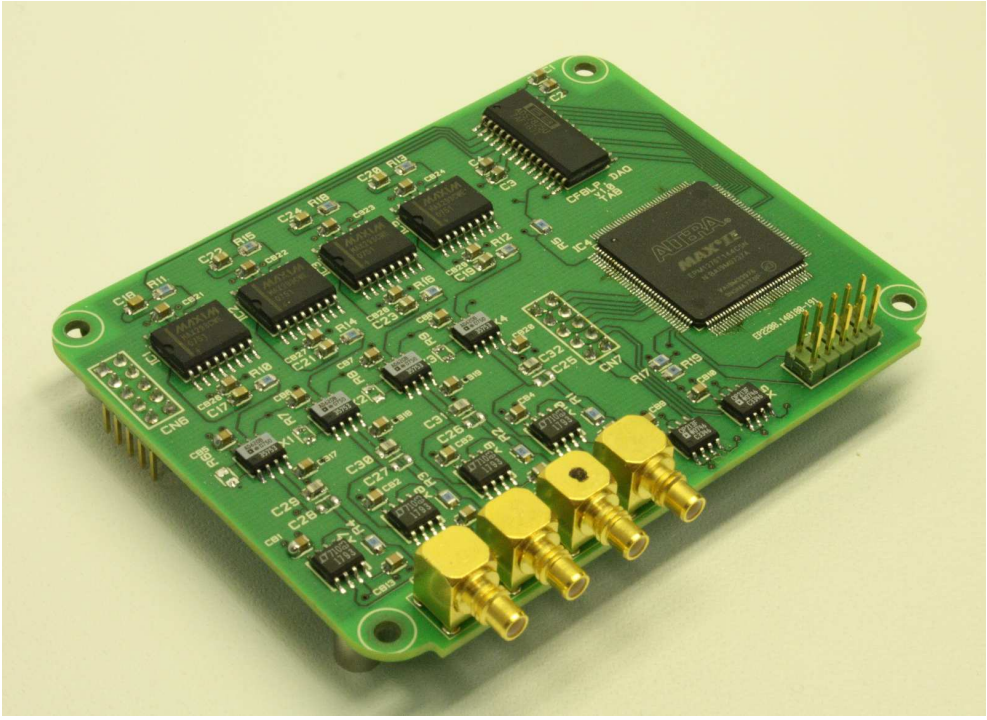

Figure 5.9: Data acquisition PCB.

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Figure 5.9 shows the top side of the DAQ PCB. The only components that are mounted on the back side are the bypass capacitors for the CPLD.

Figure 5.10 shows the signal flow from the probes to the ADC. The signal goes through current-to-voltage (I-V) conversion, differential amplification with unity gain to remove the probe bias and an anti-aliasing low pass filter before entering the ADC.

Front-End

The front-end electronics include two main components; a current-to-voltage converter and a unity gain amplifier (buffer). From the Power/Interface PCB the four probe bias voltages are generated from a 10 V voltage reference, and a following voltage divider consisting of two resistors. This is not a good supply, so; the bias voltage goes into the non-inverting input on the buffer amplifier. The bias voltage will then be put on the braid/shield of the needle probe, as a driven shield (bootstrap). Since the non-inverting input of the I-V

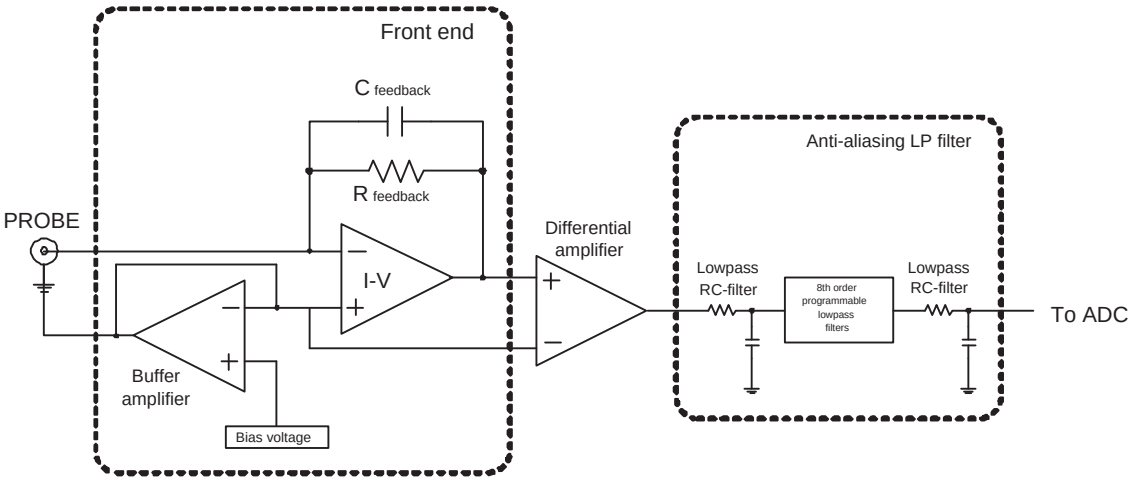
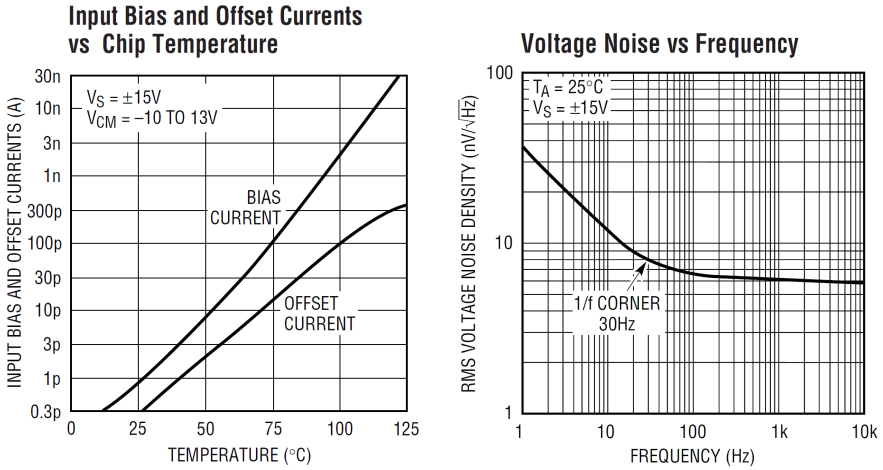


Figure 5.10: Front-end for the DAQ card

converter is not grounded, the bias voltage will act as a virtual ground. This makes the bias voltage available on the inverting input on the I-V converter, connected to the probe. For the m-NLP system the OP213 op-amp is used as the buffer amplifier, due to its low noise and low drift characteristics.

According to section 4.3, the lowest possible signal level for the JFET Input Op-Amp LT1793 is in the range of 30 - 40 pA, with a feedback resistor of 5 MΩ. This is with a signal-to-noise ratio (SNR) of about 1, which is in the lower limit of what can be characterized as a good measurement. From section 5.1 (General requirements) the lowest current that needs to be measured is defined to be 1 nA. This shows that the LT1793 is very well suited for the transimpedance amplifier, due to its low noise performance. It also has very low bias offset current and low 1/f noise, as shown in Figure 5.11. Since the LT1793 has no voltage gain, only current-to-voltage conversion through $R_{feedback}$, it gets unstable. To stabilize the LT1793 a 10 nF capacitor $C_{feedback}$ is placed in parallel to the feedback resistor $R_{feedback}$, see Figure 5.10.

In general the largest contribution to the noise throughout the system comes from the front-end electronics. For noise reduction, front-end electronics is therefore the most sensitive components regarding noise.

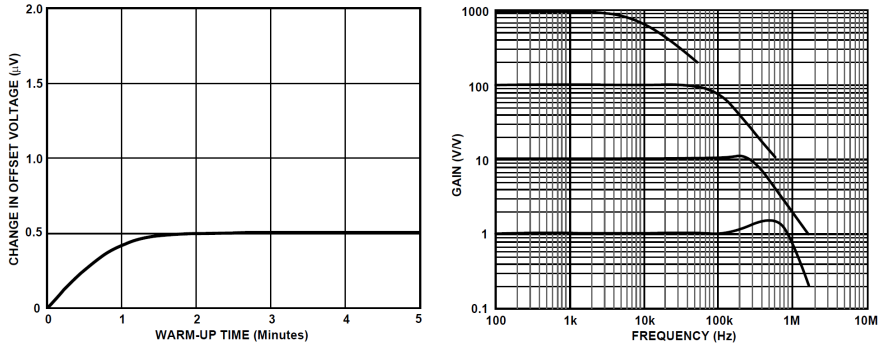


(a) Bias and offset current (b) Voltage noise

Figure 5.11: Bias and offset current, and voltage noise for LT1793

Differential amplifier

After I-V conversion, the probe signal is fed into an AD620 instrumental amplifier on the non-inverting input. The probe bias level is fed into the inverting input. This subtracts the bias voltage from the signal, giving just the collected signal from the probe on the output. To achieve a best possible signal-to-noise ratio, the AD620 is operated with unity gain.



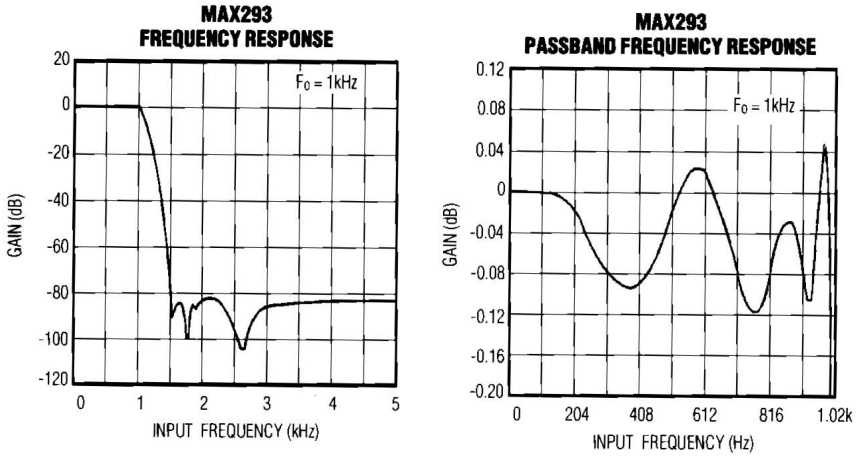
(a) Input Offset Voltage vs. Warm-up time (b) Gain vs. Frequency

Figure 5.12: Temperature stability and gain for AD620

As seen in Figure 5.12, the AD620 has excellent temperature stability when it comes to input offset voltage. The main reason why it was chosen is it's gain stability that is flat up to 100 kHz for a unity gain configuration.

LP-Filtering

After the differential amplifier, the signal goes through a LP-filter. For maximum flexibility, the MAX293 8th-Order, lowpass elliptic switched capacitor filters were used for anti-aliasing filtering. These filters operates such that the cut-off frequency f_c is set by supplying the filter with a clock having a frequency equal to $f_c \cdot 100$. The configuration for ICI-2 required a cutoff at $f_c = 1852$ Hz, making the filter clock input equal to 185200 Hz (1/18th of the SCLK frequency). To be sure that the filter's clock signal is not affecting the measured signal, passive RC-filters are put before and after the MAX293 curcuit. These are first order RC-filters, with at cutoff frequency of 10,64 kHz. This ensures that the probe signal passes through without damping, while any contamination from the filter clock is removed. A drawback with the switched capacitor filters is that they use much power, about 760 mW pr. filter. This gives a total power consumption of about 3 watts for the filters. Since the DC-DC converter can deliver up to 4.1 watts, and the rest of the electronics uses about 0.5 watt, they were chosen due to their big advantage with the programmable cut-off frequency.



(a) Frequency response (b) Gain vs. Frequency

Figure 5.13: MAX293 Operating characteristics

Figure 5.13 shows the filter characteristics for MAX293 with $f_c = 1$ kHz. The stopband is damped with more than 80 dB, and the passband ripple is less than 0.15 dB. It can be operated with a cut-off frequency range from 0.1 Hz - 25 kHz. The ratio between the cut-off frequency f_c and the stopband frequency f_s for the MAX293 filter is given by:

$$\frac{f_s}{f_c} = 1.5 \tag{5.1}$$

It was considered to use an FPAA (Field-Programmable Analog Array) for anti-aliasing filters. However, because of a small number of internal resources per package it would have demanded several FPAAs. This would have occupied too much space on the PCB, and the power consumption per FPAA was also very large. Therefore FPAAs turned out to be a bad solution and was discarded.

Analog-to-Digital Conversion

For Analog-to-Digital Conversion (ADC) a 4-channel, successive approximation 16-bit sampling CMOS A/D converter (ADS7825) is used. It utilizes four multiplexed channels, and have the following construction:

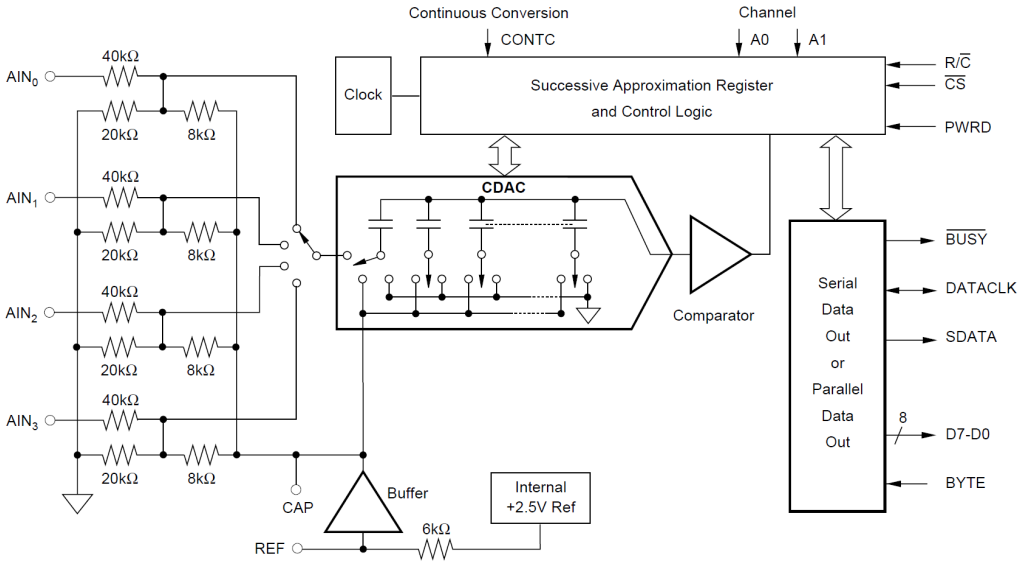


Figure 5.14: ADS7825 Schematics

The REF input is connected to ground through a 1 μF tantal capacitor, to give a stable ground level independent of noise in the ground plane. The AD7825 operates with a input range of ± 10 V, giving that:

$$LSB = \frac{20V}{2^{16}} \approx 0.305 \text{ mV/bit} \tag{5.2}$$

The I-V converter uses a feedback resistor R_f of 4.7 $M\Omega$. As the digitalized value from the ADC represents the collected current, the instrument's current resolution ΔI is given by:

$$\Delta I_{min} = \frac{0.305mV}{4.7M\Omega} = 65 \text{ pA} \tag{5.3}$$

The MAX293 LP-filters have a maximum output of ±5 V. This means that the range used for the ADC is equal to 15 bits, giving a non-optimal SNR.

Conversion time for each channel is 20 μs, and acquisition time is 5 μs. This gives a complete cycle of 25 μs for each channel. When the time for data readout is added, a complete cycle for all four channels is about 107 μs. This gives a maximum sample frequency f_s of about 9.3 kHz. This can be considered as "simultaneous sampling" of the four measurement channels, taken into account the very small translational and rotational movement of the rocket during a cycle time of about 27 μs. Figure 5.15 shows the timing diagram for the start of data conversion and serial data readout from the ADS7825 ADC.

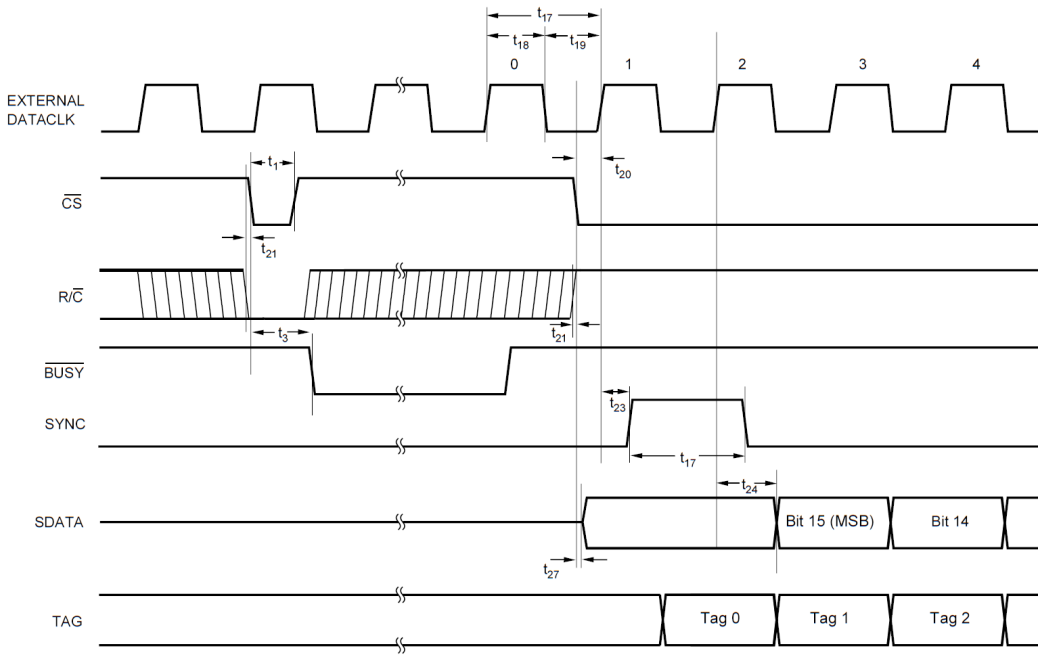


Figure 5.15: ADS7825 timing diagram for data acquisition and serial data readout (read after conversion)

Programmable Logic

To design the digital logic, the programming language VHDL was used. The program code is found in appendix C.2.

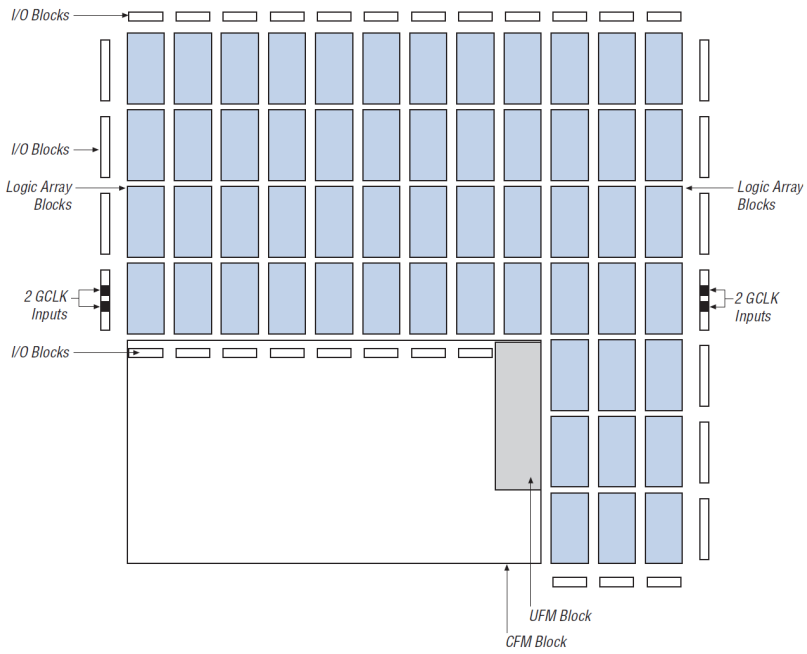


Figure 5.16: The layout of the MAX II CPLD. Flash memory is in the bottom left corner, while the rest of the chip consists of Logic Array Blocks (LAB). Connections between logic array blocks are programmable.

The CPLD chosen for the m-NLP DAQ board is an Altera MAX II EMP1270, in 144-pin TQFP (Thin Quad Flat Pack) size. It has 1270 logical elements (LE), and 116 input/outout (I/O) pins. It's internal operating voltage is 1.8 V, but it accepts a supply voltage between 2.5 V and 3.3 V. This is due to an internal linear voltage regulator in the package.

The internal flash memory in EMP1270 is divided into two sections. One CFM-block (Configuration Flash Memory) and one UFM-block (User Flash Memory). The configuration for the circuit is saved in the CFM-block. At power-up, the flash memory loads the logic into the chip. The UFM-block contains 8192 bits for general purpose storage, for example storage of vital parameters in case of a powerdown. An overview of the MAX II CPLD architecture is shown in Figure 5.16. As seen in this figure, the CPLD consists of logic array blocks (LAB), each consisting of 10 LE's. The architecture of one LE is shown in Figure 5.17.

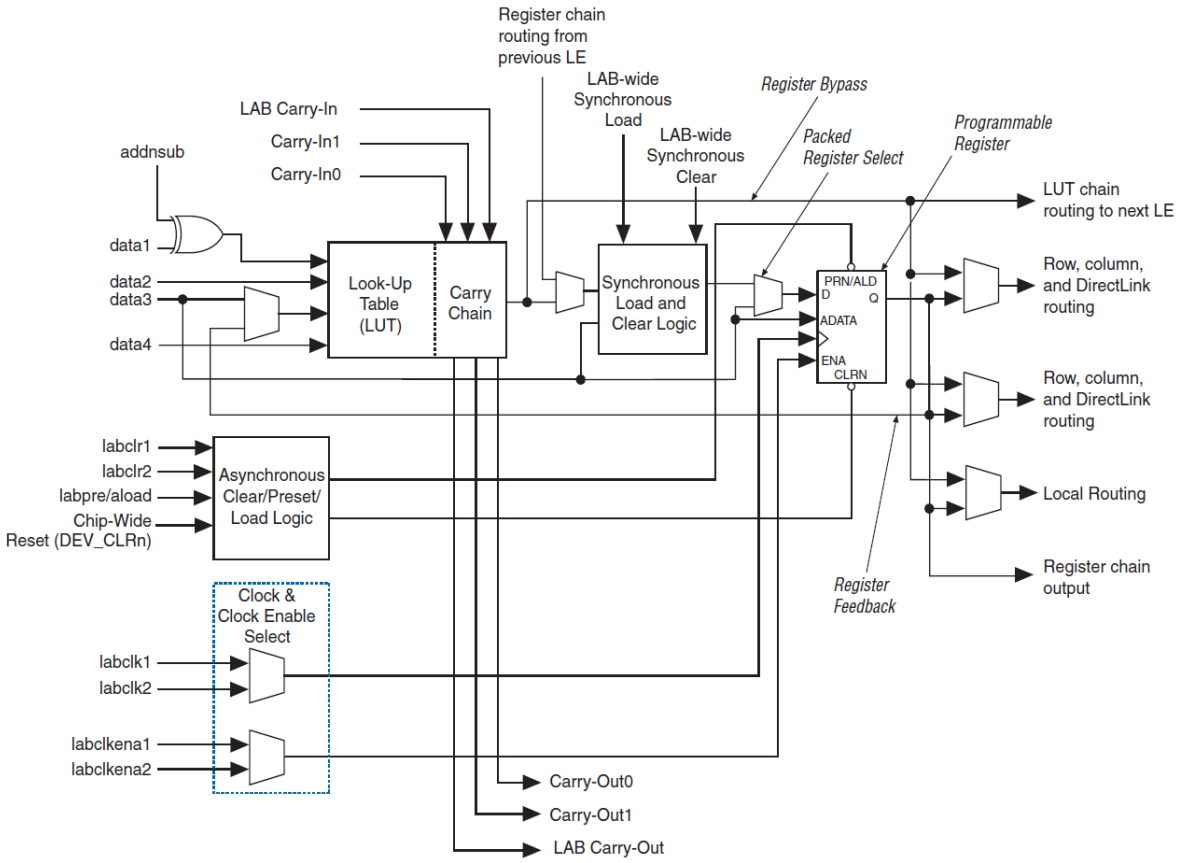


Figure 5.17: MAX II LE (Logic Element)

Further information regarding the MAX II EMP1270 architecture can be found in Altera (2006).

The CPLD has 12 power pins, and each of them is connected to a bypass capacitor. They have been placed on the back side of the board, to make signal routing easier. As recommended by Altera (2006) an 100 μF tantal capacitor is placed on the 3.3 V supply, for LF-bypassing. The CPLD supports programming over JTAG (Joint Test Action Group) interface, and a dedicated connector for JTAG is placed close to the CPLD. As specified, the JTAG TCK pin has an 1 $k\Omega$ pull-down resistor to ground, an the TMS pin has an 10 $k\Omega$ pull-up resistor to 3.3 V. Unused pins on the CPLD is not connected, since they internally will be connected to ground when the circuit is programmed.

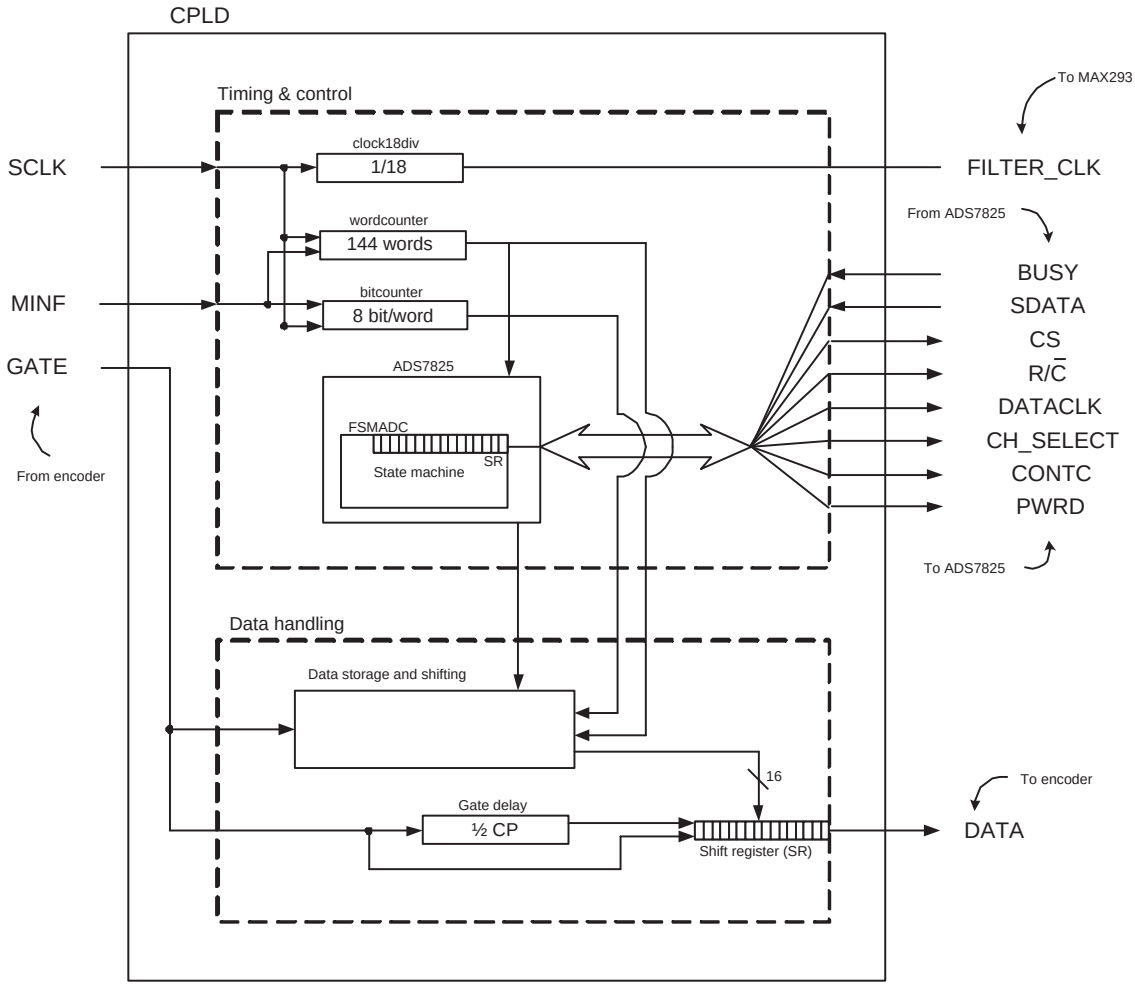


Figure 5.18: Block diagram for the digital logic

For an overview of the digital logics operation, the simplified signal flow in the CPLD is shown in Figure 5.18. The different components have the following functions:

clock18div This clock divider (1/18) outputs the filter clock to the MAX293 anti-aliasing filters.

wordcounter Count the words, for synchronization against encoder.

bitcounter Count the bits, for synchronization against encoder.

ADS7825 Controls the ADS7825. Contains the finite state machine (FSMADC), control logic and a serial to parallel shift register (SR_SerIn_redge).

Data storage and shifting Stores the measurement data, to avoid that new data overwrites data that has not yet been sent.

Gate delay Delays the gate signal from the encoder by 1/2 clock period (CP), in order to ensure correct reading of output bits on the DATA line.

Inside the ADS7825 component in Figure 5.18 a finite state machine (FSM) is used to control the ADC. The flowchart for this FSM is shown in Figure 5.19:

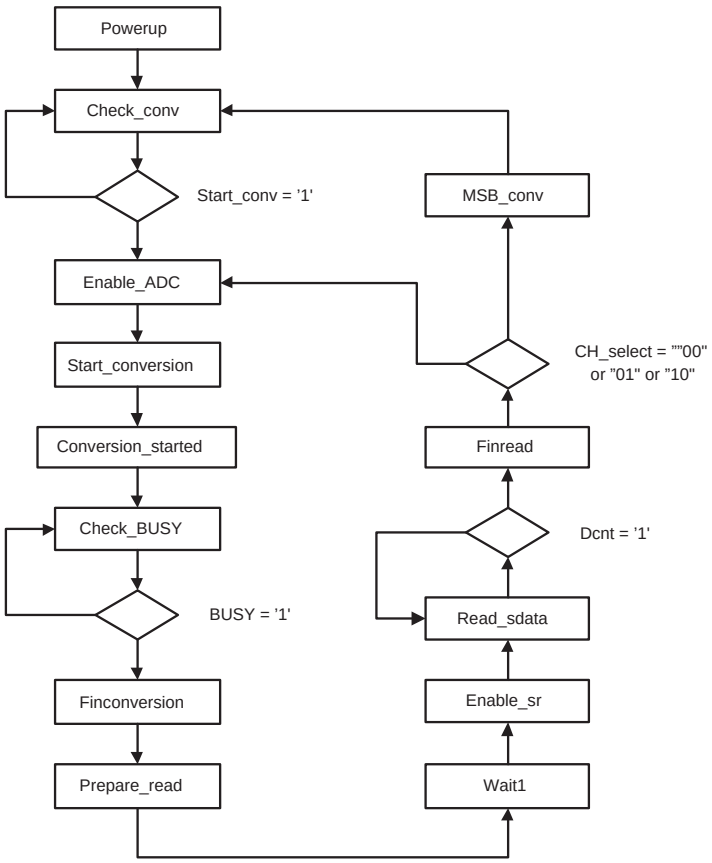


Figure 5.19: Flowchart showing the state transitions for the ADC control

Block Diagram

A block diagram of the instrument is shown in Figure 5.20.

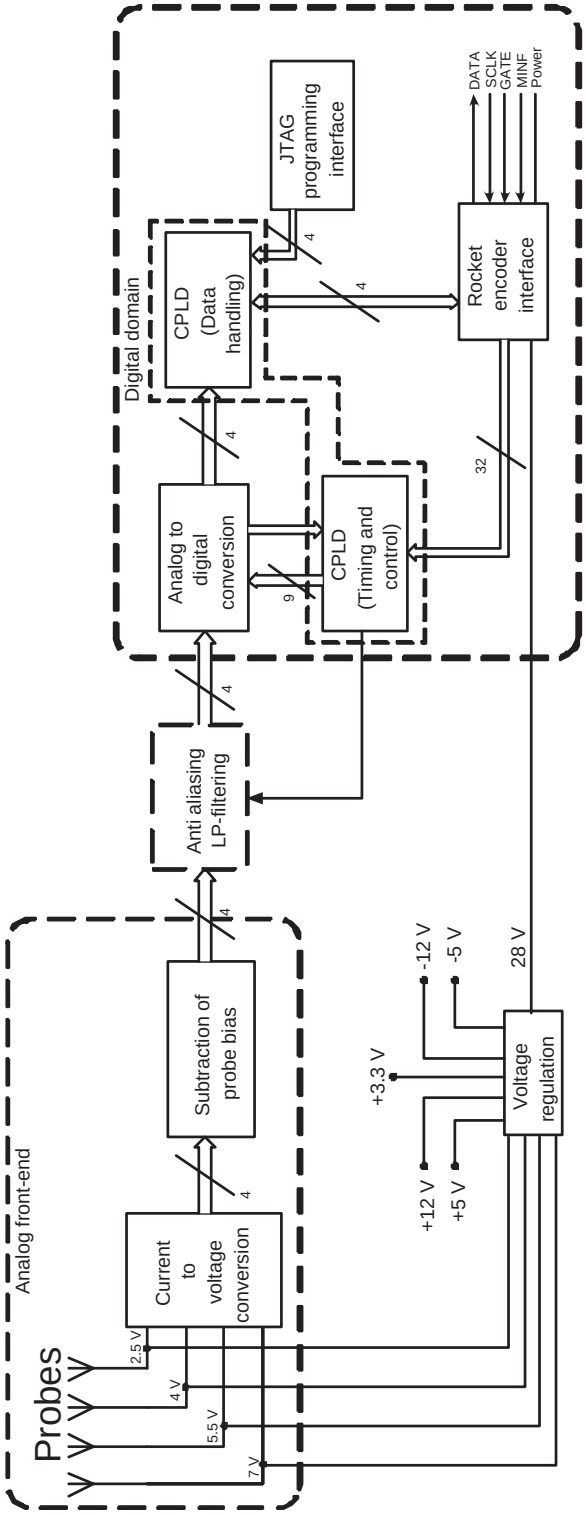


Figure 5.20: Signal flow in the DAQ unit

5.3.3 PCB design

This section describes some of the most important principles when it comes to bypassing and component placement, and how this was solved in the PCB design.

5.3.4 Ground planes and electrical noise

The more complex a circuits gets, "clean" ground gets more and more important. Ground is also referred to as the reference level which the components in the system defines as 0 V. This makes it important to have the same ground potential throughout the circuit. Analog components are especially vulnerable to ground noise. One solution is to have separate ground planes for the analog and digital part of the system, implemented by multi-layer PCBs.

The components which contributes most to noise in the system are the digital components. For that reason some say that it is favorable to separate the ground plane into an analog and a digital part. On way of doing this is using a slit only giving a narrow connection bridge between the analog and digital domains of the ground plane (Grødal, 1997). As a result of this, the digital circuits will affect the analog circuits less. The main problem with this solution is that signals can unintentionally be routed across the split in the ground plane. This causes the return current in the ground plane to travel a long path to pass through the bridge between the two domains. This may also cause additional interference from digital electronics on analog electronics. If the return currents are allowed to go beneath the signal currents, the return current will in most cases follow close to this path. This happen because high frequency signals sees this at the path with lowest obstructiveness (lowest inductance). According to Ott (2001) it is recommended not to split the ground plane, but instead design the card with the analog and the digital part separated from each other by clever component placement. This approach was chosen in this work. Both of the m-NLP cards use multi layer PCBs with separated analog and digital domains. Good placement of the components gave a low noise in the system.

5.3.5 Bypass capacitors and electrical noise

Digital components are operating in a pulsed mode. This gives transient current pulses for two main cases. A short circuit shock from V_{cc} to ground when the input changes value, and the current peak when the output is driven to a new value. Both events will draw a significant current from the power

supply. These effects can cause transient voltage drops in V_{cc}, and generate noise that transmit into the ground plane.

To avoid these effect, the solution is to add bypass capacitors to have a buffer in the supply inputs that handles these transients. The sharp transient will then be handled by the capacitor, drawing current much slower from the power supply. This increases the stability of the system, and removes much load from the power supply. The transient currents will still be present, but they are no longer a problem for the rest of the circuit. The two types of bypassing is HF (high frequency) and LF (low frequency). HF bypassing is used for protection against transient currents. LF bypassing is used to stabilize low frequent voltage variations from the power supply. A normal value for HF bypass capacitors is 100 nF, and for LF bypass a value of 1 - 100 μF is often used. For LF bypass capacitors it is common to use electrolytes, often tantal capacitors, due to their good low frequency performance. For HF bypassing ceramic capacitors are used since they have good high frequency characteristics.

To preserve a "clean" ground and a stable voltage supply the bypass capacitors must be placed as close as possible to the corresponding component. Ideally the bypass capacitors should be placed between the connection to power / ground and the component. The ideal placement of the bypass capacitor is on the same side as the IC is mounted, since this gives the shortest signal path. If space is a problem, it is a solution to place the bypass capacitor on the back side of the PCB. Then vias has to be used in the PCB for connections to ground (Gnd) and V_{cc}, see Figure 5.21. However, this is usually not the optimal solution.

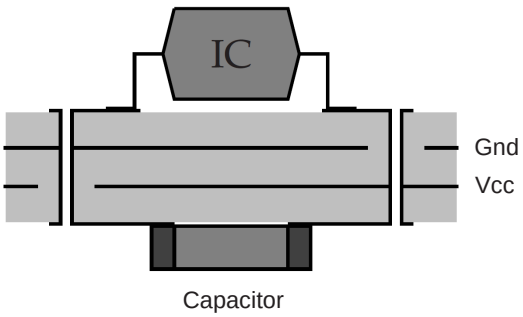


Figure 5.21: Capacitor placed on the opposite side of the IC. This is a non-ideal placement, since connections to GND and V_{cc} is between the IC and the capacitor. The advantage is short lanes, which simplifies placement close to the IC.

When placing bypass capacitors, the main goal is to obtain a cleanest possible ground. This gives a requirement to place the bypass as close to the ground connection as possible (see Figure 5.22). The optimal solution is to route the power and ground distribution such that power and ground connections enter the pad on the bypass capacitor on one side, and exits on other side. This ensures that no current can go around the capacitor. In this work this "rule" had to be circumvented for the CPLD's bypass capacitors. Because the CPLD has a very large number of I/O lines the capacitors had to be placed on the back side of the PCB, in order to maintain sufficient routability of the PCB. Due to problems with the Cadstar PCB design tool the second via to the capacitor pad, which is needed for a theoretically correct connection, was automatically removed. All other components besides the CPLD have bypass capacitors placed in correspondence to the correct placement as described by Grødal (1997) and reviewed in this section. This means that the bypass capacitors are placed as close to the ground connection pin as possible, as shown in Figure 5.22.

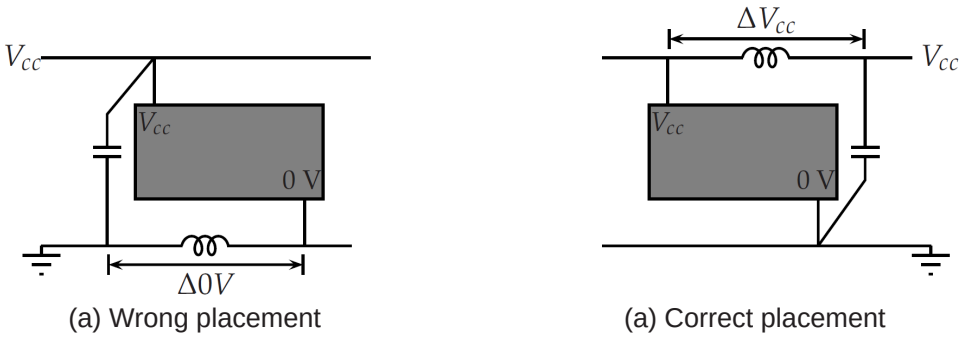


Figure 5.22: IC placement, as described in Grødal (1997). Because of the inductance in every conductor, a voltage difference in the conductor will occur in case of transient currents. Therefore, the conductors have to be as short as possible. In (a) the voltage variation on V_{cc} will be zero, while the voltage variation will occur on ground. In (b) the noise from the transient currents will occur on V_{cc}, while ground stays "clean")

5.3.6 m-NLP Specification

The specifications for the m-NLP system (electronics and probes) are given in Table 5.2

Weight (electronics)	130 grams
Weight (box)	250 grams
PCB size	$9.4 \cdot 6.9\ cm^2$
Measurement channels	4
External system clock	Up to 10 MHz
Sample frequency	Up to 9 kHz
Measurement range	Down to about 100 pA
Resolution	16 bits
A.A. filter transition ratio	1.5
Current consumption	122 mA @ 28 V (3.5 W)
Accepted supply voltage	8.4 V to 36 V
Data interface	Serial (RS422)

Table 5.2: m-NLP specifications

Chapter 6

Calibration and Testing

6.1 Probe Testing

Access to ESA lab facilities was granted through ESA PRODEX Arrangement No. 90335. The goals for the performed tests were to check the dimensions and behavior for the probes, and to verify that the measurement principle worked (confirm that $I^2(V)$ gives a straight line). The interesting density range was from $n_e = 10^{-9}\ m^{-3} - 10^{-12}\ m^{-3}$. The probes had a diameter of 0.51 mm and a length of 25 mm. For these probes the specified density range corresponds to a current from the probes ranging from 1 nA to 1 μA. The technical testing was conducted to confirm that the preliminary design of the preamplifier could be used on the flight-version of the rapid sampling Langmuir probe electronics.

6.1.1 Experimental Setup

In the plasma tank laboratory at ESTEC the probes were placed on a 200 mm long boom produced at the mechanical workshop at UiO. The boom was supported inside the tank by a rotating rod going up to the centreline of the tank; see Figure 6.1. The boom was made to make it possible to mount the probes, separated by a sufficiently large distance such that the two probes do not interfere with each other. The expected Debye shielding length inside the chamber for the used probe dimensions were 2 - 5 cm. The rod was made from aluminium, and the braid on the probes was isolated from the rod by a plastic encapsulation around the mounting holes in the rod.

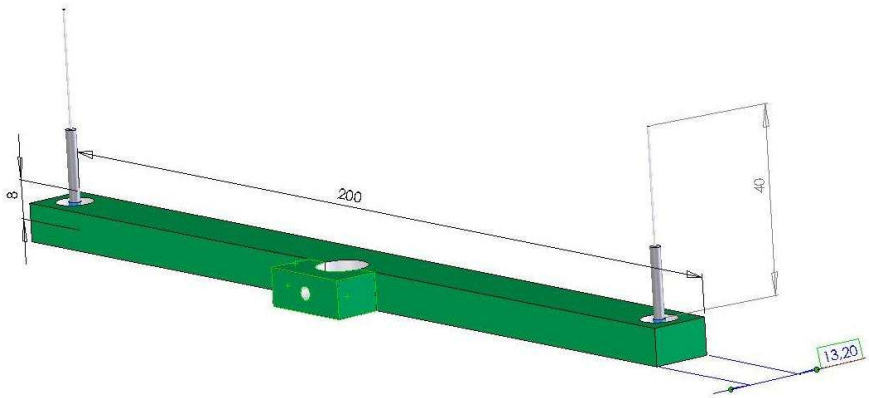


Figure 6.1: Mechanical size of mounting structure for two m-NLP probes. All dimensions are in mm.

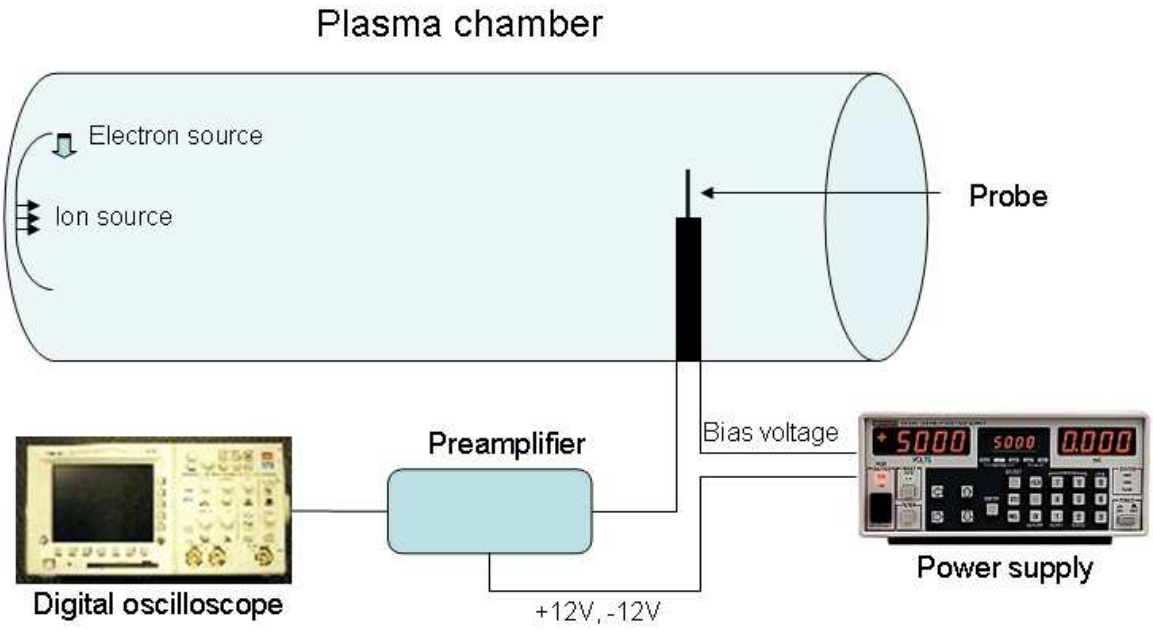


Figure 6.2: Sketch of the measurement setup

As seen in Figure 6.2, the probes were put in the horizontal plane, centered in the plasma chamber. The probes were connected to the preamplifier via a two channel coaxial cable throughput at the top of the chamber. Cable

lengths were about 4 meters. Supply voltage for the preamplifier was $\pm 12V$, and an adjustable voltage supply for probe biases were used. The electron density n_e inside the chamber was given by the technical personnel at ESTEC to be between $6 \cdot 10^{10}\ m^{-3}$ and $8 \cdot 10^{10}\ m^{-3}$.

6.1.2 Test Results

Voltage settings for the probe bias levels were chosen from 0.125 V to 6 V, in steps of 1 V from 1 V and above. Beneath 0.125 V it was impossible to get a solid readout, because of the noise in the plasma. Above 6 volts the preamplifier went into saturation (output above ± 12 volts). This was because of the amplification of the noise in the plasma. The measurements were conducted with about 15 seconds between each readout (the plasma was assumed to be stable). The two probes were not sampled simultaneously, since the oscilloscope with noise averaging only had one input. Figure 6.3 shows the plotted results from the measurements taken in the plasma tank. The measured current is shown as a function of the applied probe bias voltage.

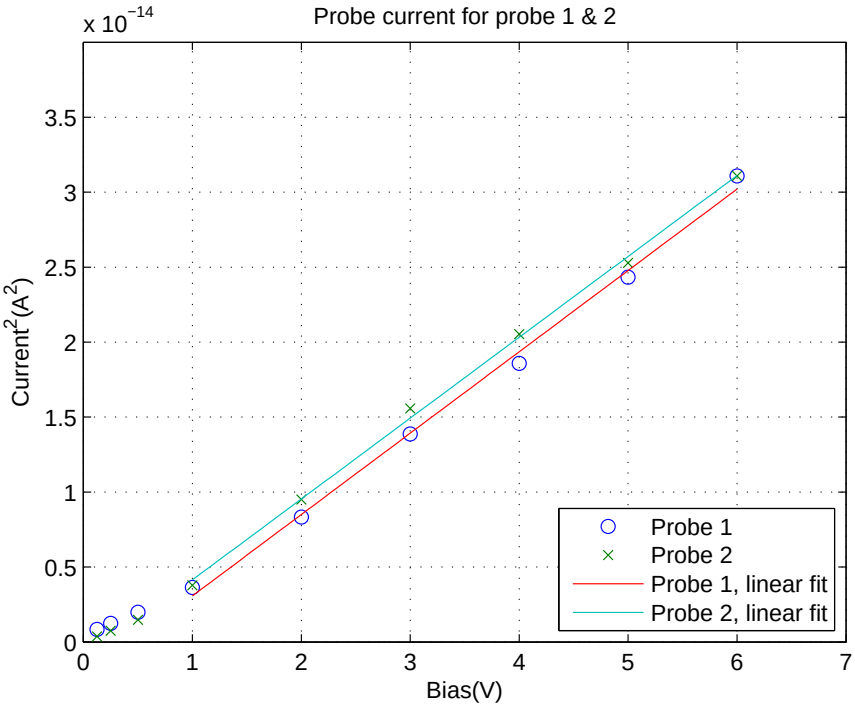


Figure 6.3: Results from the tests in the ESTEC plasma chamber

As seen in Figure 6.3 there is a linear relation between the applied bias voltage and the current squared. From chapter 3 this result shows that the probe configuration is well suited for the m-NLP measurement concept. The measurements showed concurrent data for the two probes, with just small deviations above 1 V. There was an absence of filtering in the preliminary instrument, and significant oscillations in the plasma tank. Therefore readout below 1 V in bias level was discarded in the linear fitting due to noise.

The equation for the calculation of electron density based on measurements from two probes biased at different potential is given in Eq.(3.5). The value of the constant K is

$$K = \sqrt{\frac{m}{2q(q2rl)^2}} = 9.3 \cdot 10^{17}[(\frac{kg}{C^3 m^4})^{-1}] \tag{6.1}$$

For the ICI-2 probes we have the following numbers:

- m = $m_e = 9.10938188 \cdot 10^{-31}$ kg
- q = $q_e = 1.60217646 \cdot 10^{-19}$ C
- r = probe radius = 0.51 mm
- l = probe length = 25 mm

This gives according to Eq.(3.5) the following densities for the two probes:
Probe 1:

$$\begin{aligned} n_e &= 9.3 \cdot 10^{17}[(I_{e2}^2 - I_{e1}^2)(V_2 - V_1)]^{1/2)} \\ &= 9.3 \cdot 10^{17}[(3.021 \cdot 10^{-14} - 0.307 \cdot 10^{-14}/(6-1)]^{1/2} \\ &= 6.85 \cdot 10^{10} m^{-3} \end{aligned} \tag{6.2}$$

Probe 2:

$$\begin{aligned} n_e &= 9.3 \cdot 10^{17}[(I_{e2}^2 - I_{e1}^2)(V_2 - V_1)]^{1/2} \\ &= 9.3 \cdot 10^{17}[(3.111 \cdot 10^{-14} - 0.414 \cdot 10^{-14}/(6-1)]^{1/2} \\ &= 6.83 \cdot 10^{10} m^{-3} \end{aligned} \tag{6.3}$$

These results correspond very good to the expected n_e inside the plasma chamber. This was estimated to be between $6{\cdot}10^{10}$ m^{-3} and $8{\cdot}10^{10}$ m^{-3}. From Figure 6.3 it can be seen that the two probes gave a data set with almost the same gradient for the linear fit. The numbers in Eq.(6.2) and Eq.(6.3) have

a deviation of about 0.3%. This indicates that the measurement principle works very well. Since it was unknown if the plasma was symmetric, the probes positions were swapped. This gave similar results for the two probe positions, indicating an almost symmetric plasma.

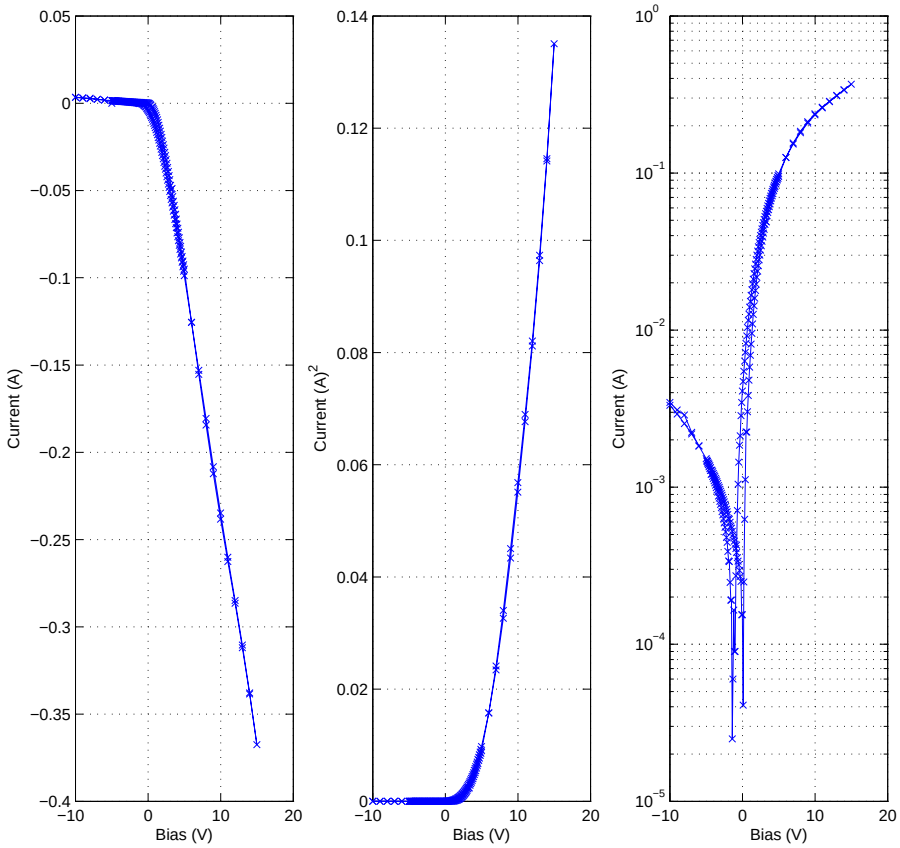


Figure 6.4: Hysteresis from bias voltage sweep

In addition to investigating the linearity of the probes, a second test of the probes was conducted in October 2008 by Jean-Pierre Lebreton from ESA at ESTEC. The test checked if the probes had any hysteresis when the bias voltage was swept. Figure 6.4 shows that the probes have a small hysteresis. This will not influence the measurements of the m-NLP system, since a fixed bias will be applied.

6.2 Instrument Testing and Calibration

This section will deal with the calibration of the electronics, and the results from the calibration.

6.2.1 Test and Calibration Setup

The calibration conducted in the lab facilities at the University of Oslo was done by connecting the m-NLP DAQ unit to an PCM encoder from Forsvarets Forskningsinstitutt (FFI). Data readout from the instrument was made by a PCM decoder from Eidel. The FFI PCM encoder was identical with the encoder used in the ICI-2 payload. All data were extracted and analyzed in Matlab. For current stimuli a Keithley Model 2635 Single-channel Low Current System Source Meter Instrument was used to input the current in steps of 10 nA. Hold-time for each step was 0.2 seconds, and the current range was from 1 pA to 1 μA.

6.2.2 Test and Calibration Results

The midrange for each channel, with deviation from normal midrange of data value 32768, is shown in Table 6.1. Midrange values are based on the output from the system with no signal on the probes, when the rocket was on the launcher and running on internal power.

Channel	Midrange	Deviation	Deviation (nA)
1	32263	505	32.8
2	32252	516	33.5
3	32247	521	33.8
4	32300	468	30.4

Table 6.1: Midrange for each channel

As seen in Table 6.1 there is a significant bias on each channel, requiring a calibration of the instrument.

In Figure 6.5 the measured current is plotted as a function of the input current to the system. The bottom plot shows the residuals between the linear fit and the input current steps. Throughout the range the residuals stay the same, indicating a linear output from the system if the input current had been a linear sweep; not a step response. The calibration model used is given by

$$I_{meas} = \alpha \cdot I_{true} + \Delta I \tag{6.4}$$

where I_{meas} is the measured current from the instrument, I_{true} is the stimuli current from the current source, α is the scale factor and ΔI is the current offset. The measured current I_{meas} is calculated from the decoder systems digital output value DV by

$$I_{meas} = \frac{DV \cdot \frac{20\ \mathrm{V}}{2^{16}}}{R_f} \tag{6.5}$$

where $R_f = 4.7\ M\Omega$ is the feedback resistor. For channel 1 on the instrument, the calibrated data gave the following results for α and ΔI:

$$\begin{aligned} \alpha &= 1.02 \\ \Delta I &= 6.46 \cdot 10^{-10}\ \mathrm{A} \end{aligned}$$

For the other three channels the result is very similar, and with very good linearity. The norm of residuals shown in Figure 6.5 is a measure of the goodness of fit, where a smaller value indicates a better fit than a larger value.

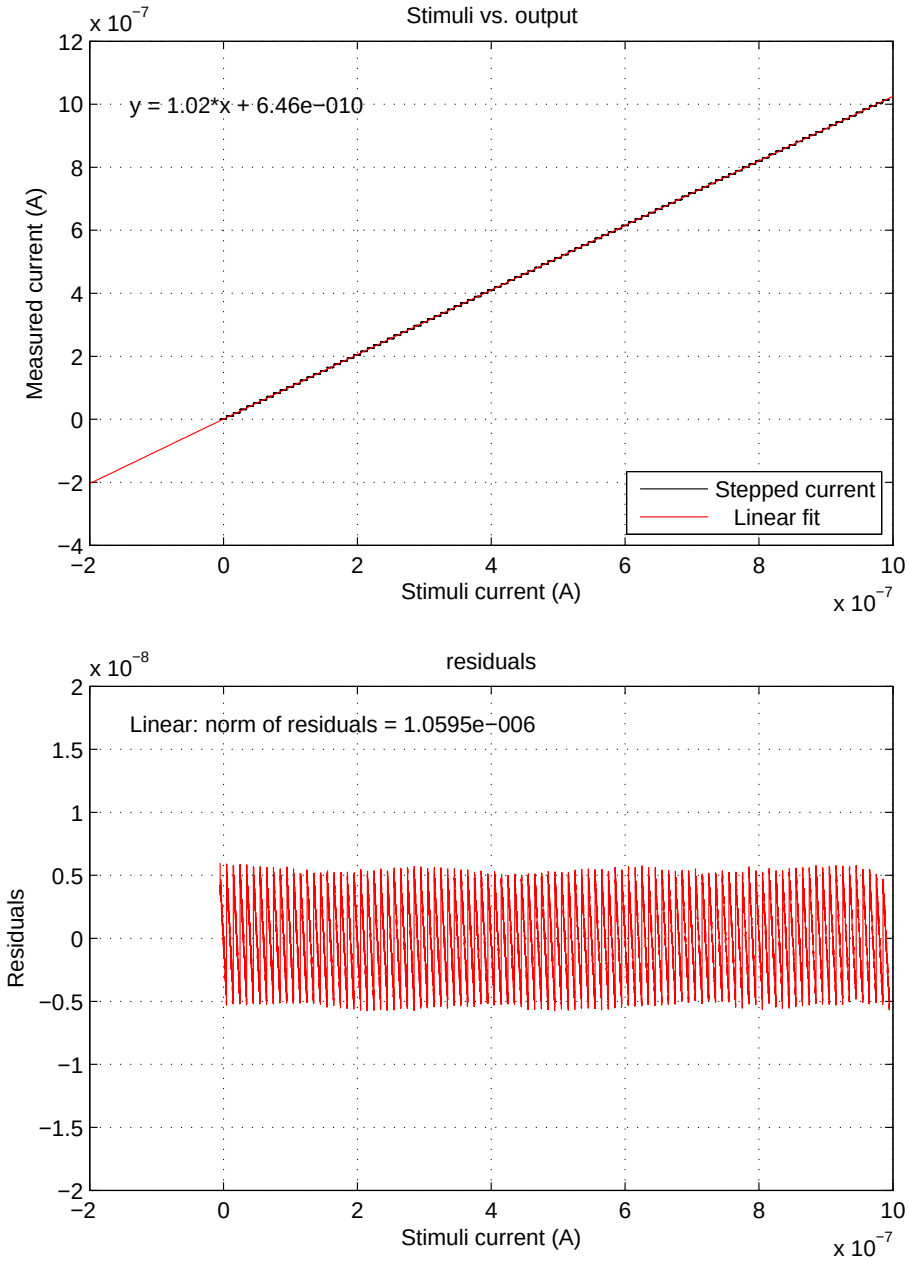


Figure 6.5: Linearity including residuals for the DAQ unit

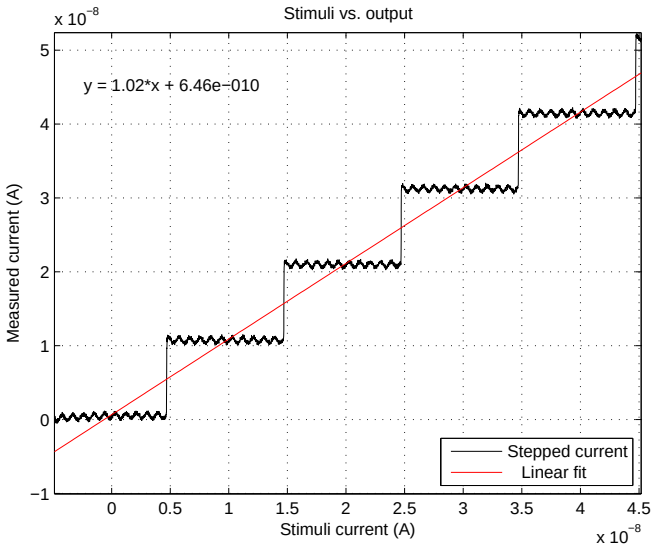


Figure 6.6: Stepped input current, and linear fit

The stimuli signal can be seen in Figure 6.6. To find the linear fit the measured data is left-shifted according the the x-axis values, such that the center value for each current step lines up with the correct stimuli current. Compensation of ICI-2 data based on the pre-flight calibration was performed by

$$I_{cal} = \frac{I_{meas} - \Delta I}{\alpha} \tag{6.6}$$

where I_{cal} is the calibrated current measurement, and α and ΔI was determined in the pre-flight calibration. After midrange correction, the current offset in the calibration model for all channels are less than 0.65 nA.

The measured frequency response of the system (for ICI-2 configuration), with a cutoff frequency of 1852 Hz, is shown in Figure 6.7 and Figure 6.8.

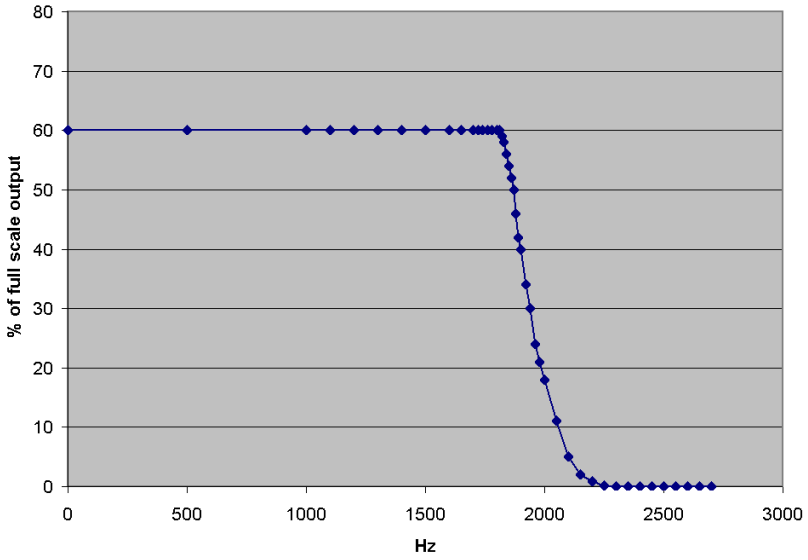


Figure 6.7: Frequency response in % of full scale output

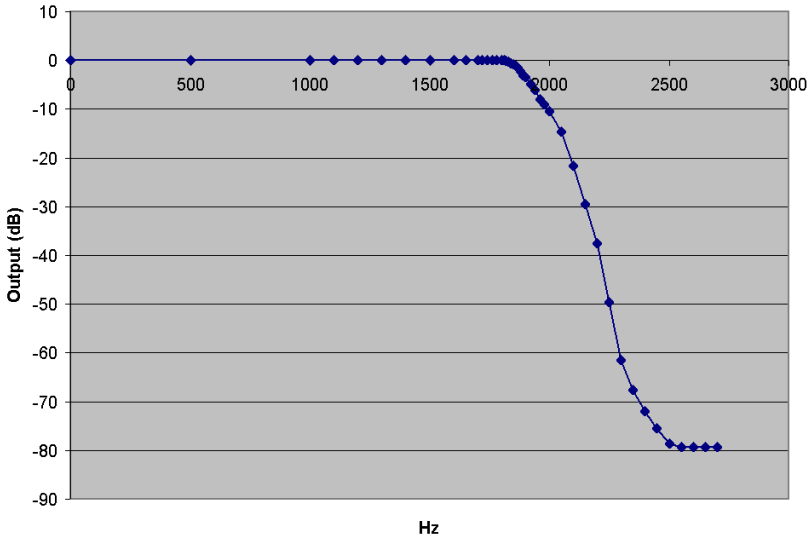


Figure 6.8: Frequency response in dB

Chapter 7

ICI-2 integrations and Rocket Campaign

The 4-NLP instrument was launched with the ICI-2 rocket (Investigation of Cusp Irregularities) from Spitsbergen, Ny-Ålesund, on 5th December 2008. The ICI-2 rocket campaign had a launch window from 28th November to 7th December 2008.

Collaboration partners in addition to the University of Oslo were Andøya Rocket Range (ARR), Institute of Space and Astronautical Science(ISAS) / Japan Aerospace Exploration Agency (JAXA) and the University of Bergen. The first integration was conducted at Andøya Rocket Range from 4th to 11th June 2008. The University of Oslo had the integration scheduled on the 16th and the 17th of June. In addition to a communication check against the rocket encoder, the instrument was integrated mechanically into the rocket. This verified that the physical measurements were inside the specified limits. The next integration milestone was the 2nd integration and environmental testing at Packforsk AB in Stockholm, 1st to 11th of September 2008. Here the payload was tested according to NASA test levels according to the Sounding Rocket Handbook; see Table 7.1

Test item	**Test level**	**Duration (S)**
Random thrust axis	10 G rms, 20-2000Hz	60
Random lateral axes	7.6 G rms 20-2000 Hz	60

Table 7.1: Vibration test criteria (according to NASA Test levels according to Sounding Rocket Handbook)

Additionally the payload was temperature cycled once from -20^oC to $+45^oC$ and four times from 0^oC to 40^oC.

The m-NLP instrument successfully "passed" all vibration en environmental tests. The last integration was conducted at Svalrak in Ny-Ålesund, the ARR launch base at Svalbard. This final assembly began on 21st November, and the payload was connected to the launch vehicle on 27th November. From 28th November none of the scientific or weather conditions were met, until 5th December. At 10.35 UT 5th December 2008 the rocket was launched, and everything worked as planned. The rocket motor configuration used for the ICI-2 payload was a two-stage rocket motor configuration; a Sonda VS30 as the first stage and an Improved Orion as the second stage. The rocket reached an apogee of about 330 km, and the total flight time was 574 seconds. It is shown in chapter 8 that the instrument worked as intended.

Figure 7.1: ICI-2 mission badge

Chapter 8

Flight Data Analysis and Results

On the 5th of December 2008 at 10.35 UT the ICI-2 sounding rocket was launched from Ny-Ålesund, Svalbard. The figures in this chapter shows the collected data from the m-NLP instrument, and interprets some interesting phenomena. All data are visualized in Matlab, and can be found in larger version in Appendix B.

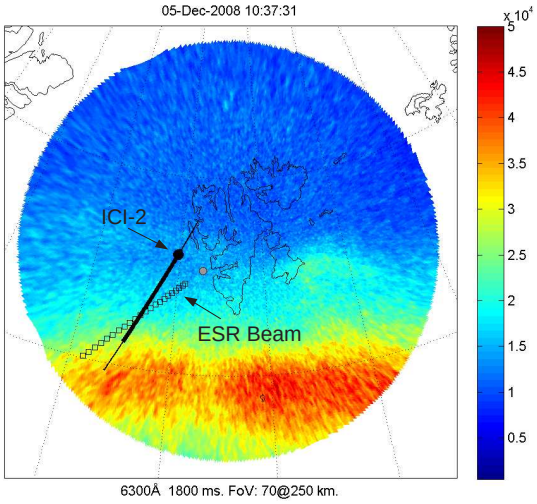


Figure 8.1: 630.0 nm all-sky image projected onto a geographic map. The straight black line represents the rocket trajectory, where the thick part of it depicts when it was above 200 km altitude. The other line represents the pointing direction of the EISCAT Svalbard Radar (ESR) that intersected the rocket trajectory at 200 km down leg

Figure 8.1 shows an image of the auroral 630.0 nm oxygen emission taken at 10:37.31 UT, i.e. 140 seconds after launch. The position of the rocket at that time is marked by the black dot on the black line depicting the trajectory. At that time the entire trajectory was straddled with auroral emissions.

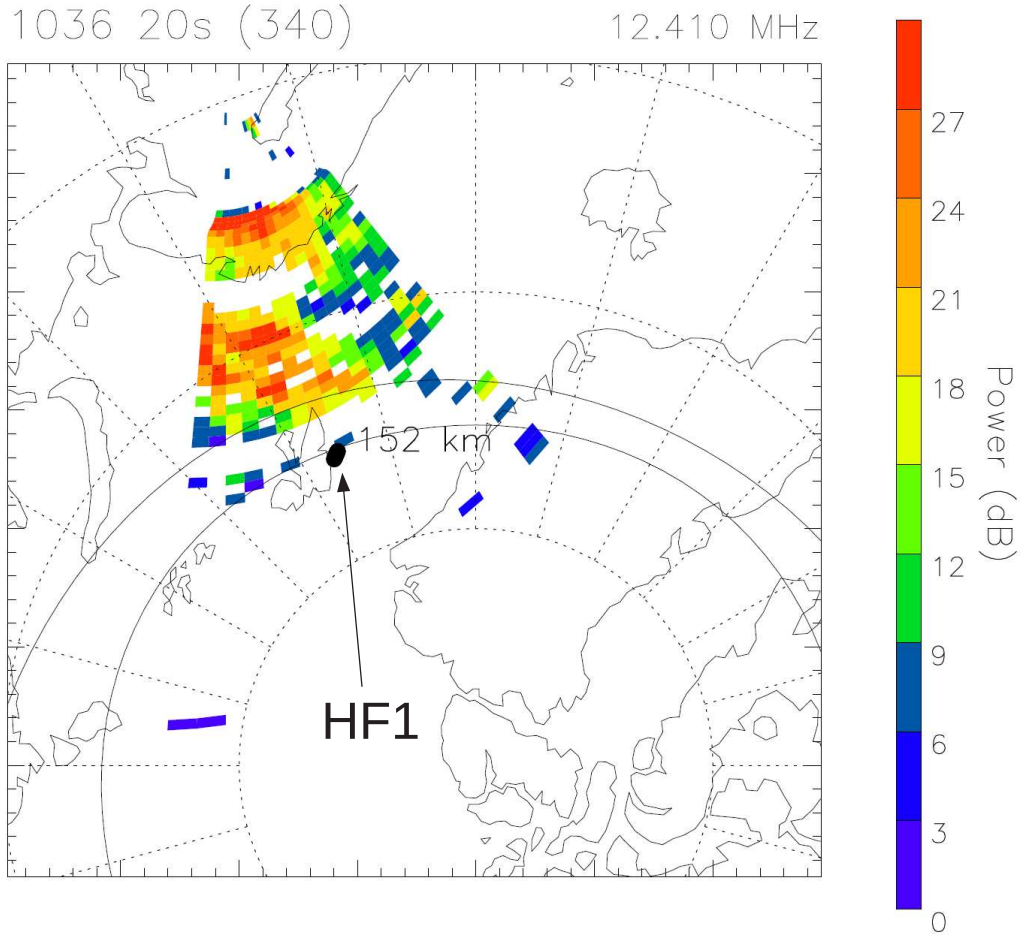


Figure 8.2: Radar power density plot showing the rocket's first encounter with HF backscatter targets

Figure 8.2, Figure 8.3 and Figure 8.4 shows CUTLASS HF radar data. There are three encounters with significant HF backscatter targets during the rocket flight.

Figure 8.5 shows the raw data for all four channels during the entire flight. Here the data values have been converted to current (in nA) in Matlab by using the calibration coefficients from section 6.2.2. It is clearly seen that the four channels biased at different voltage levels produce higher output with

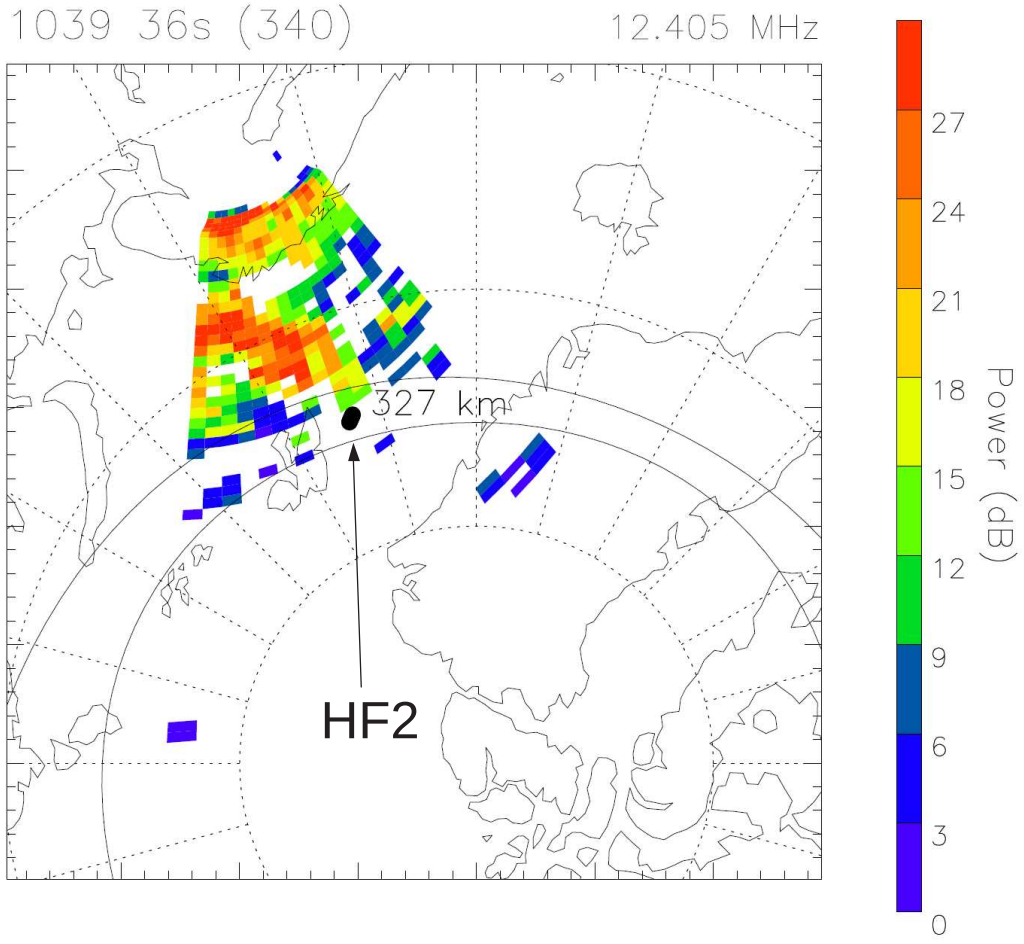


Figure 8.3: Radar power density plot showing the rocket's second encounter with HF backscatter targets

increasing bias.

When examining the data, it was seen that the output from measurement channel 4 was too high, and deviated from the linear fit for measurement channel 1 - 3. The most likely reason is that the bias voltage has been higher than 7.0 V. During the integration tests in Ny-Ålesund the bias voltages were checked, and probe 4 was verified to have a bias voltage of 7.0 V. After a look into the electronics design, the most probable reason would be that the resistor R13 on the Power and Interface PCM were detached due to the vibrations during launch. Another possible explanation is expansion of bubbles in the solder during the pressure decrease, causing the solder to tear apart. In order to test this "hypothesis", resistor R13 (see Appendix A.2)

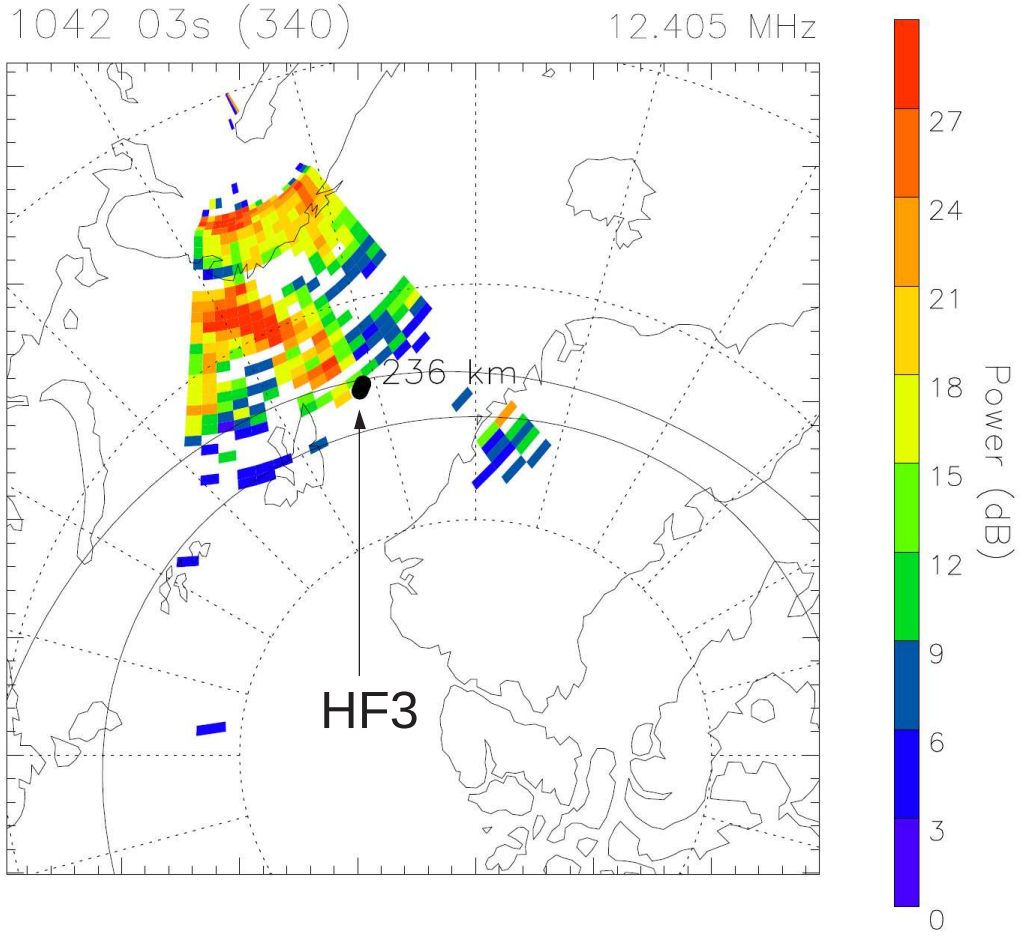


Figure 8.4: Radar power density plot showing the rocket's third encounter with HF backscatter targets

was removed from the spare unit. This breaks the ground connection in the voltage-divider behind the AD587 voltage reference, making the voltage to the probe biasing equal to 10 V. To check the linearity of the output with both 7.0 V and 10.0 V on probe 4, the data set was sent through a correlation filter, checking linearity at both bias voltages. If the output from the filter is equal to 1, the data points should be on a straight line. This work was done in collaboration with PhD student Knut Stanley Jacobsen.

Figure 8.6 shows that a bias voltage of 10.0 V on probe 4 gives a correlation coefficient of 1 for almost the entire flight after nose cone separation. This is a good indication that 10.0 V is the correct bias value. The rest of the figures in this chapter is therefore based on the following bias voltages:

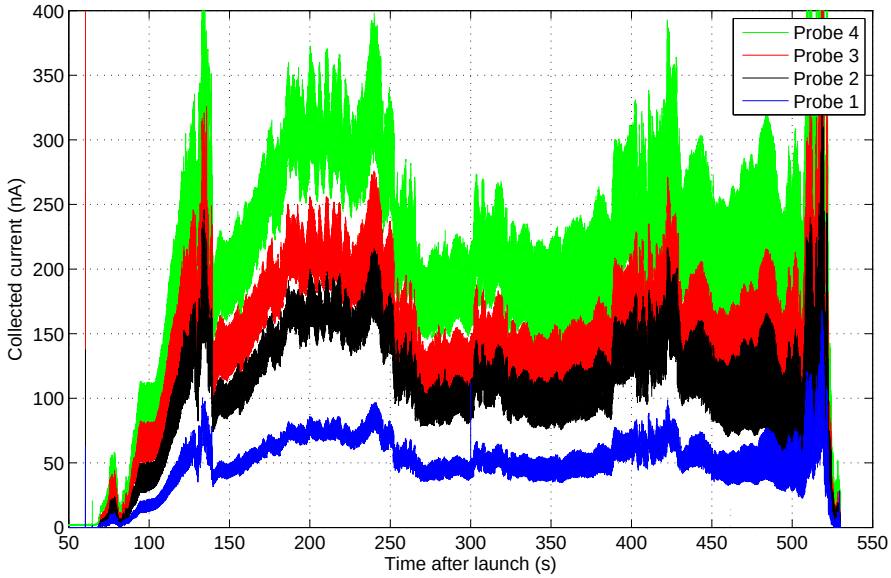


Figure 8.5: The expected parallel curves

2.5 V, 4.0 V, 5.5 V and 10.0 V. This underlines the importance of having redundancy in the number of probes. In the perfect case only two probes are required, while we used four probes.

Figure 8.7 shows a spin disturbance for all measurement channels. This is expected, since the ICI-2 rocket is spin stabilized. The spin frequency f_{spin} of the rocket is about 3.27 Hz, and it is stable throughout the entire flight. Therefore, it can easily be removed by filtering the signal with a narrow banded band-reject filter centered around f_{spin}.

Figure 8.8 shows the unfiltered data, together with the filtered data from a band-reject filter from 3.07 Hz to 3.47 Hz, with a transition bandwidth of 0.2 Hz. After filtering, a frequency of $2 \cdot f_{spin}$ is observed. This is caused by the geometry of the probes, as seen in Figure 5.3. Since the rocket for most of the flight will have an angle between its center axis and the plasma it goes through, the probes will pass through four "regions" in one revolution. When the probe is in the position where it is in front of the bowshock, it will measure undisturbed plasma. When it has rotated 180 degrees from this position, it is positioned so that it sees wake effects from the fixed bias Langmuir probe experiment from ISAS/JAXA. When it has rotated 90 degrees and 270 degrees corresponding to its initial position, it will have the the same conditions. This gives a periodic signal with frequency $2 \cdot f_{spin}$. This can be

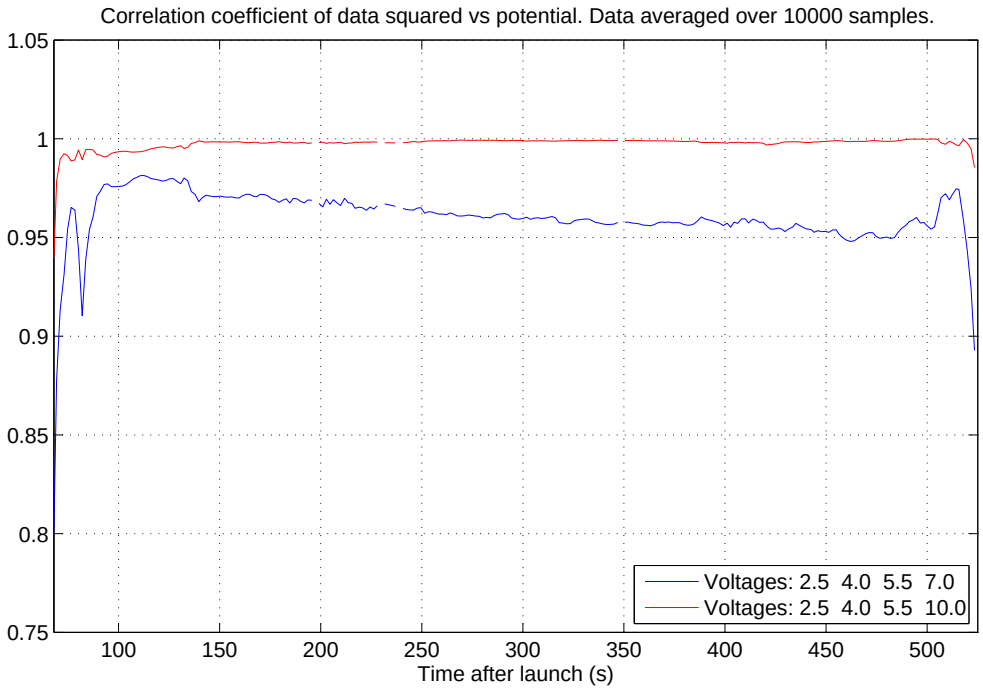


Figure 8.6: Correlation coefficient for the four probe voltages

removed from the signal with another band-reject filter at $2f_{spin}$.

In figure 8.9 the combined data from all four probes are shown, as calculated by Eq.(3.5). The electron density for the entire flight is mostly between $n_e = 10^{10}$ and 10^{11} m^{-3}, with some peaks above 10^{11} m^{-3}. The encounters with HF backscatter targets are market by HF1, HF2 and HF3.

One of the goals for the ICI-2 mission was to measure fine-structures in the ionospheric plasma. Figure 8.10 reveals a 10 ms plasma structure just prior to 138.7 which corresponds to a 10-15 meter spatial structure in the plasma. A more accurate estimate will be possible when the data from the DC electric field has been analyzed, as we need to determine the actual plasma drift relative to the rocket.

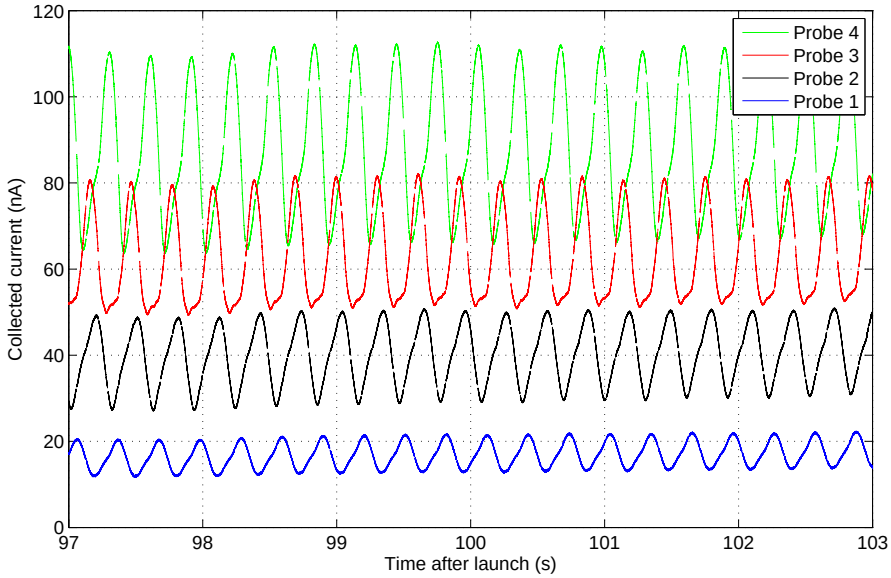


Figure 8.7: Spin disturbance

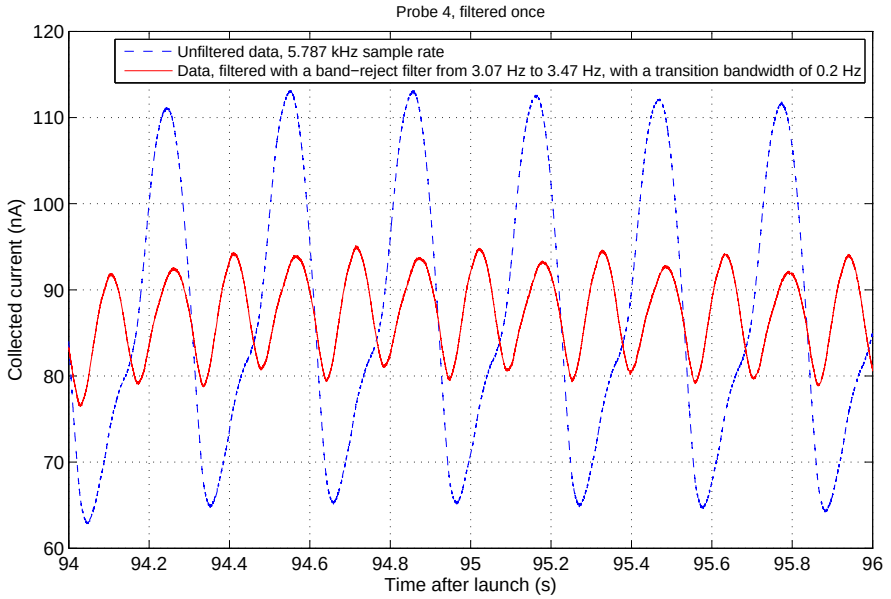


Figure 8.8: Spin disturbance at 2x spinrate, due to boom geometry

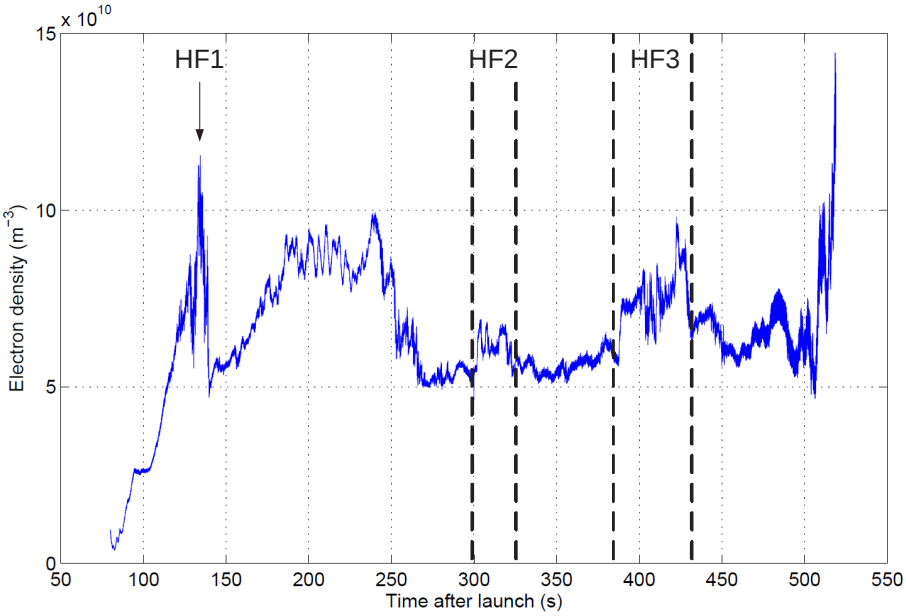


Figure 8.9: Processed data from the entire flight

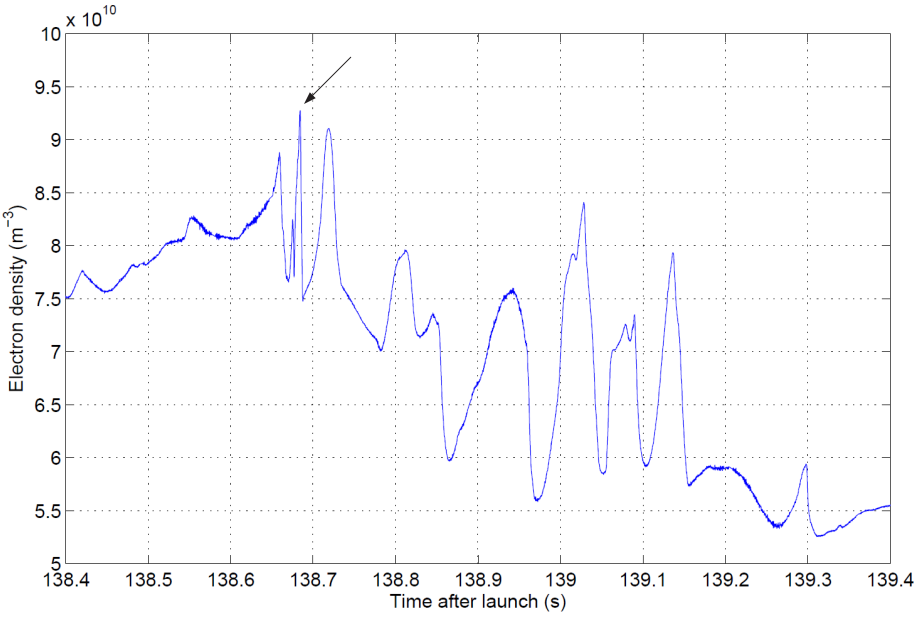


Figure 8.10: 1 second of high-resolution data reveal a 10 ms structure indicated by an arrow just prior to 138.7 s of flight time

Chapter 9

Summary and Conclusions

This chapter sums up the work presented in this thesis. It reviews the main contributions and results, and directions for further work are identified.

9.1 Conclusions of the Present Work

The work of this masters thesis has been related to instrument development for the ICI-2 sounding rocket. The thesis describes the design, development and analysis of a novel multi-Needle Langmuir Probe System. According to the accomplishments and contributions, the following conclusions are drawn:

- A novel 4-Needle Langmuir Probe (m-NLP) system has been developed, making it possible to derive the electron density with high time resolution without the need to know the electron temperature and the spacecraft potential. The system consists of four needle probes and a DAQ unit, making it possible to sample all for channels up to 9 kHz. The new Langmuir system has been verified both in the plasma chamber at ESTEC and onboard the ICI-2 sounding rocket launched from Svalbard 5th December 2008.

- A calibration station for low-current measurements has been established at UiO. A PCM encoder equal to the one used in sounding rockets from ARR is used for the. This makes it possible to check the functionality of the m-NLP system in a full operational mode, with stimuli current to the probes in the pA range.

- The functionality of the front-end current to voltage and amplification circuit has be verified in the plasma chamber at ESTEC. In addition a pre-flight calibration of the electronics showed that the calculations

for the front-end noise level was in the correct range, and the noise levels were sufficiently low to ensure good measurements in the defined measurement range for ICI-2.

- Post-flight analysis of the data generated by the instrument on the ICI-2 rocket flight have been done, verifying that the instrument worked as intended, measuring the smallest thinkable structures (electron gyro radius in the order of 10 meters) in ionospheric plasma.

9.2 Future work

Based on the experiences and results of this thesis, several improvements and changes can be implemented in future versions of the instrument. This section will also describe future projects which the probe system can or will take part in:

- The m-NLP system has been chosen to be the scientific instrument onboard CubeSTAR, one of the picosatellites in the Norwegian student satellite program.
- A possible launch on a ESA satellite in 2011-2012 is under consideration, and there is a funding possibility through the ESA GSTP programme.
- The system will be a part of the upcoming ICI-3 rocket payload, possibly with more than four measurement channels.
- To lower the current consumption on a future CubeSAT, the MAX293 programmable filters should be replaced by 6th or 8th order active Sallen-Key filters, reducing the power consumption for the anti-aliasing filtering in each channel by 80-90%.
- The ADS7825 16-bit four channel ADC can be replaced by AD7684, giving possibilities for much higher sampling rates if needed
- The AD620 differential amplifier can be replaced by AD8253 Programmable Gain Instrumentation Amplifier, with programmable gain of 1, 10, 100 or 1000. This would give the possibility to implement automatic gain control (AGC), which increases the measurement range.
- One dedicated measurement channel with a swept bias can be implemented. This will give measurements down in the retardation region,

which can supply valuable data for an estimation of the electron temperature.

- The placement of the probes should be reviewed, to avoid non-ideal effects.

Bibliography

Altera (2006). *MAX II Device Handbook*.

Bekkeng, J. K. (2002). Prototyputvikling av e-felt eksperiment for små sonderaketter. Master's thesis, University of Oslo.

Fraden, J. (2003). *Handbook of Modern Sensors: Physics, Designs, and Applications*.

Grødal, A. (1997). *Elektromagnetisk kompatibilitet*. Tapir forlag.

Milan, S., T. Yeoman, and M. Lester (1998). The dayside auroral zone as a hard target for coherent hf radars. *Geophysical Research Letters*.

Milan, S., T. Yeoman, M. Lester, E. Thomas, and T. Jones (1997). Initial backscatter occurrence statistics from the cutlass hf radars. *Annales geophysicae-atmospheres hydrospheres and space sciences*.

Moen, J., I. Walker, L. Kersley, and S. Milan (2002). On the generation of cusp hf backscatter irregularities. *Journal of geophysical researchspace physics*.

Mott-Smith, H. M. and I. Langmuir (1926). The theory of collectors in gaseous discharges. *Physical Review*.

Muralikrishna, P. and M. A. Abdu (1991). In-situ measurements of ionospheric plasma density by two different techniques - a comparison. *Journal of atmospheric and terrestrial physics* (53), 787–793.

Ott, H. W. (2001). Partitioning and layout of a mixed-signal pcb. *Printed Circuit Design*.

Pfaff, R. F., J. E. Borovsky, D. T. Young, and Editors (1998). *Measurement Techniques In Space Plasmas*. American Geophysical Union.

Power-one (2006). *IMX4 DC-DC Series Data Sheet, 4-Watt DC-DC Converters*.

Rodger, A., K. Baker, J.Dudeney, R. Greenwald, M. Pinnock, P. Newell, N. Mattin, , and C. Meng (1995). Hf radar signatures of the cusp and low-latitude boundary-layer. *Journal of geophysical research-space physics*.

Sarpeshkar, R., T. Delbruck, and C. Mead (1993, Nov). White noise in mos transistors and resistors. *Circuits and Devices Magazine, IEEE 9*(6), 23–29.

TI (2000). *Op Amps for Everyone*. Texas Instruments.

Yeoman, T., S. Milan, M. Lester, E. Thomas, and T. Jones (1997). Initial backscatter occurrence statistics from the cutlass hf radars. *Annales geophysicae-atmospheres hydrospheres and space sciences*.

Appendix A

Schematics

This appendix contains the schematics, the PCB layouts and the part lists for the electronics. The software programs Cadstar 9.0 and 10.0 from Zuken have been used.

A.1 DAQ PCB

Listing: Parts list for DAQ board

Parts List

CADSTAR Design Editor Version 10.0.0.2

Part Name	Description	Qty.	Comps.
AD–SSM/AD620AR/SMD	OPAMP INSTR.	4	X1−4
AD–SSM/OP213/SMD–S	DUAL OPAMP	2	X5−6
ALTERA/EPM1270T144C5	ALTERA MAX II 1270 CPLD	1	IC4
BB/ADS7825/SMD	4ch 16b ADC	1	IC8
CAP/100NF/SMD0805R	10% 50V 0805 X7R	39	C1 C5−16 CB1−10 CB13−24 CB26−29
CAP/10NF/SMD0805R	10% 50V 0805 X7R	8	C25−32
CAP/680NF/SMD0805R	10% 100V 0805 X7R	8	C17−24
CAP/680PF/SMD0805R	5% 50V 0805 NP0	1	C2
CAP/1u0F/SMD0805R	5% 50V 0805 NP0	2	C3−4
CON/85SMB50−0−1/	SMB–CONNECTOR	4	CN2−5
CON/STL5X2	5X2 SCOTT ELEC. PINROW	3	CN6−8
MAXIM/MAX293/SMD	8th order LP elliptic filter	4	IC1−3 IC5
RES/10K0/SMD0805R	RESISTOR KOA 0805 1% 0.125W	2	R5+R17
RES/22R0/SMD0805R	RESISTOR KOA 0805 1% 0.125W	8	R10−16+R18
RES/1K00/SMD0805R	RESISTOR KOA 0805 1% 0.125W	1	R19
RES/4M7/SMD0805R	RESISTOR KOA 0805 1% 0.125W	4	R1−4
RES/0R0/SMD0805R	RESISTOR KOA 0805 1% 0.125W	4	R6−9
SH3.0	HOLE FOR 3MM SCREW	4	SH1−4
SPES/LT1793/SMD	OP–AMP	4	X7−10

End of report

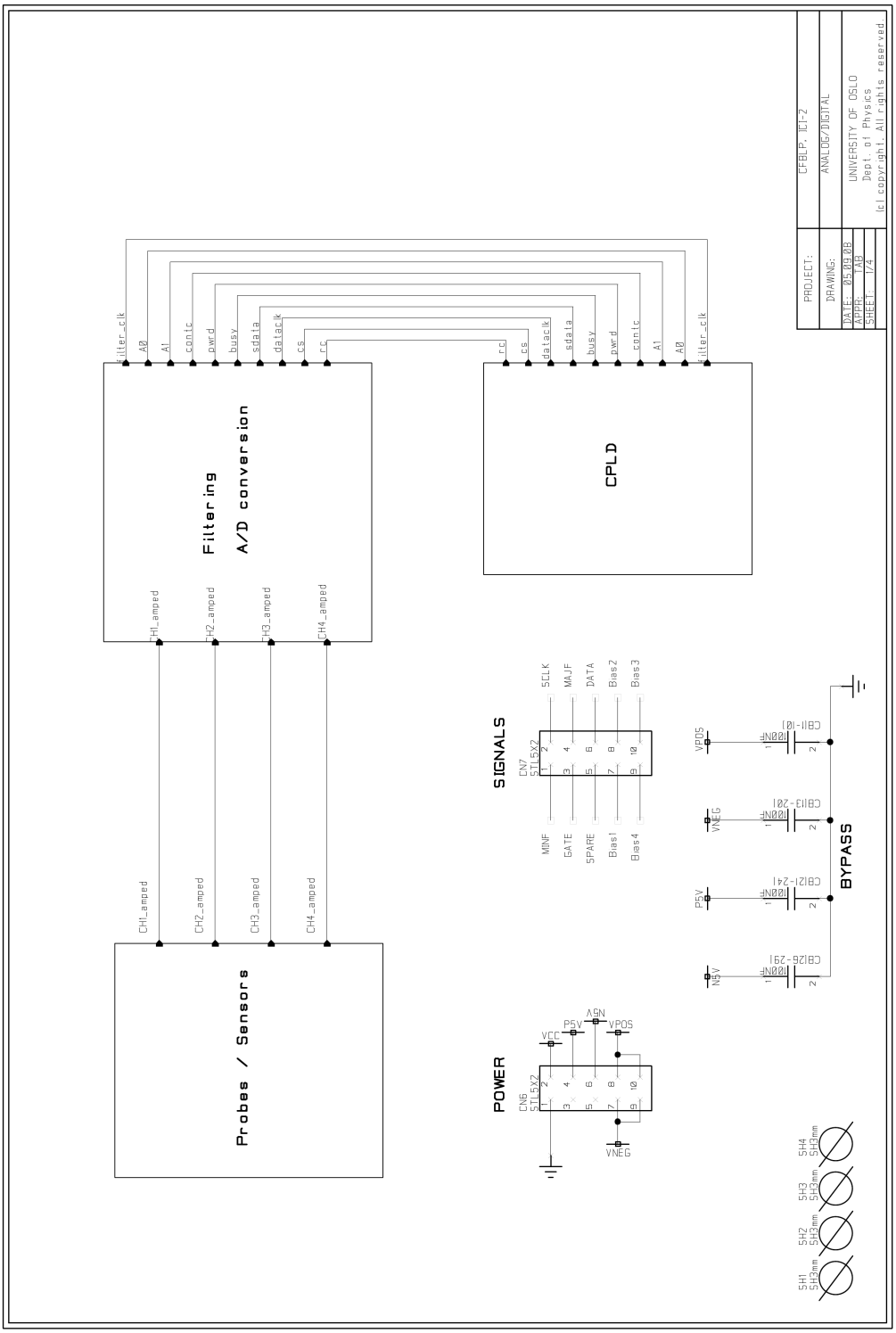


Figure A.1: DAQ card top schematics

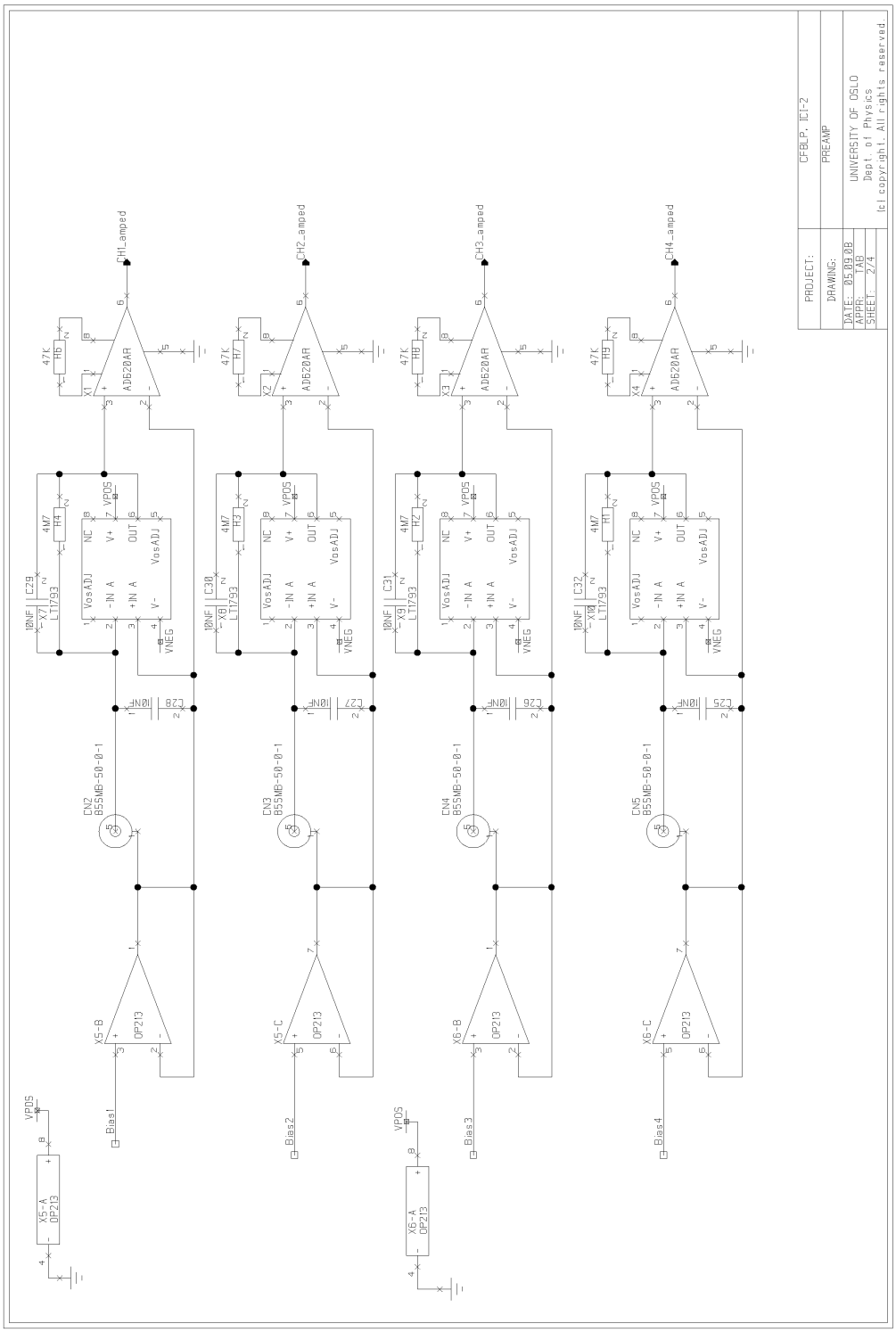


Figure A.2: DAQ card front-end

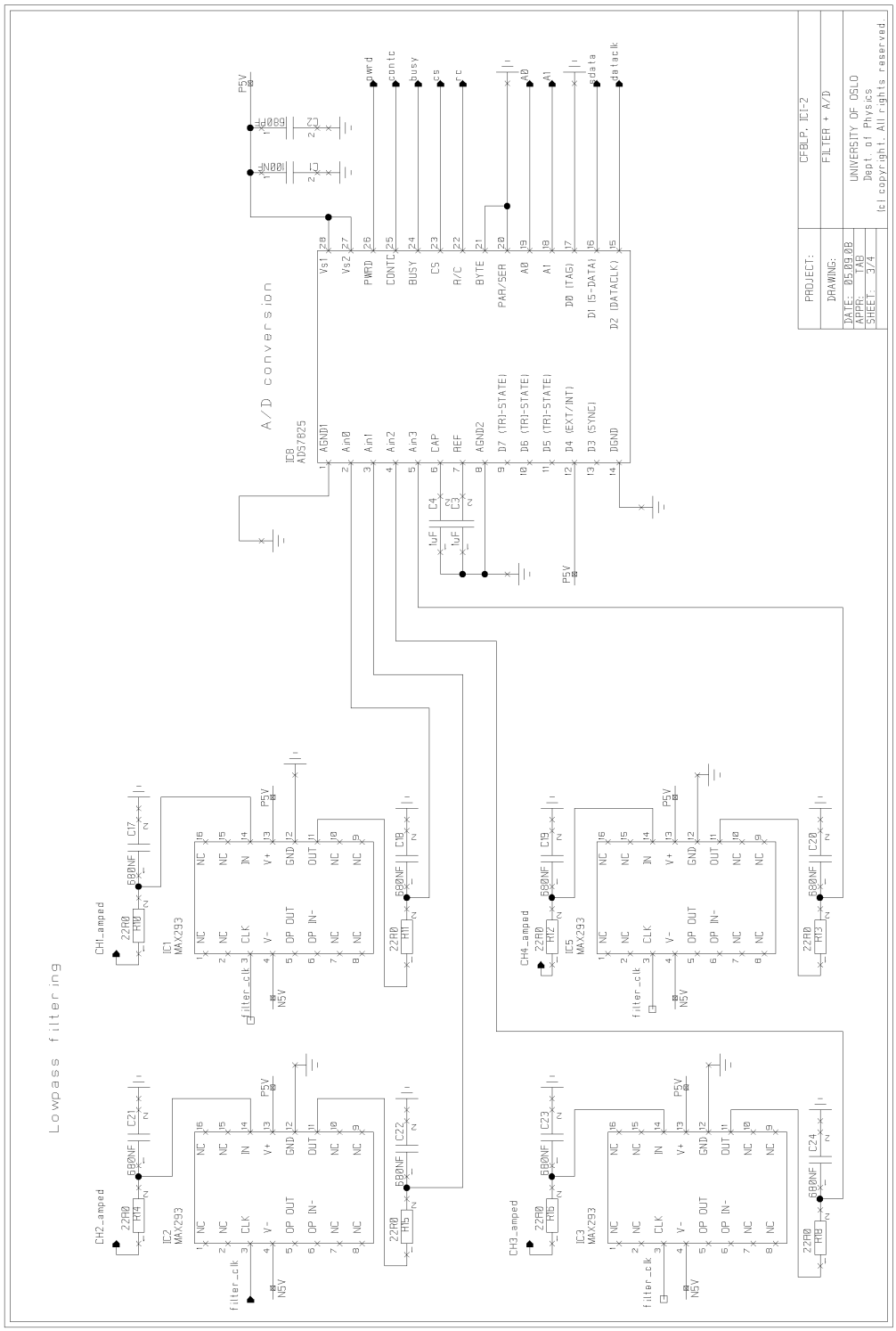


Figure A.3: DAQ card filtering and ADC

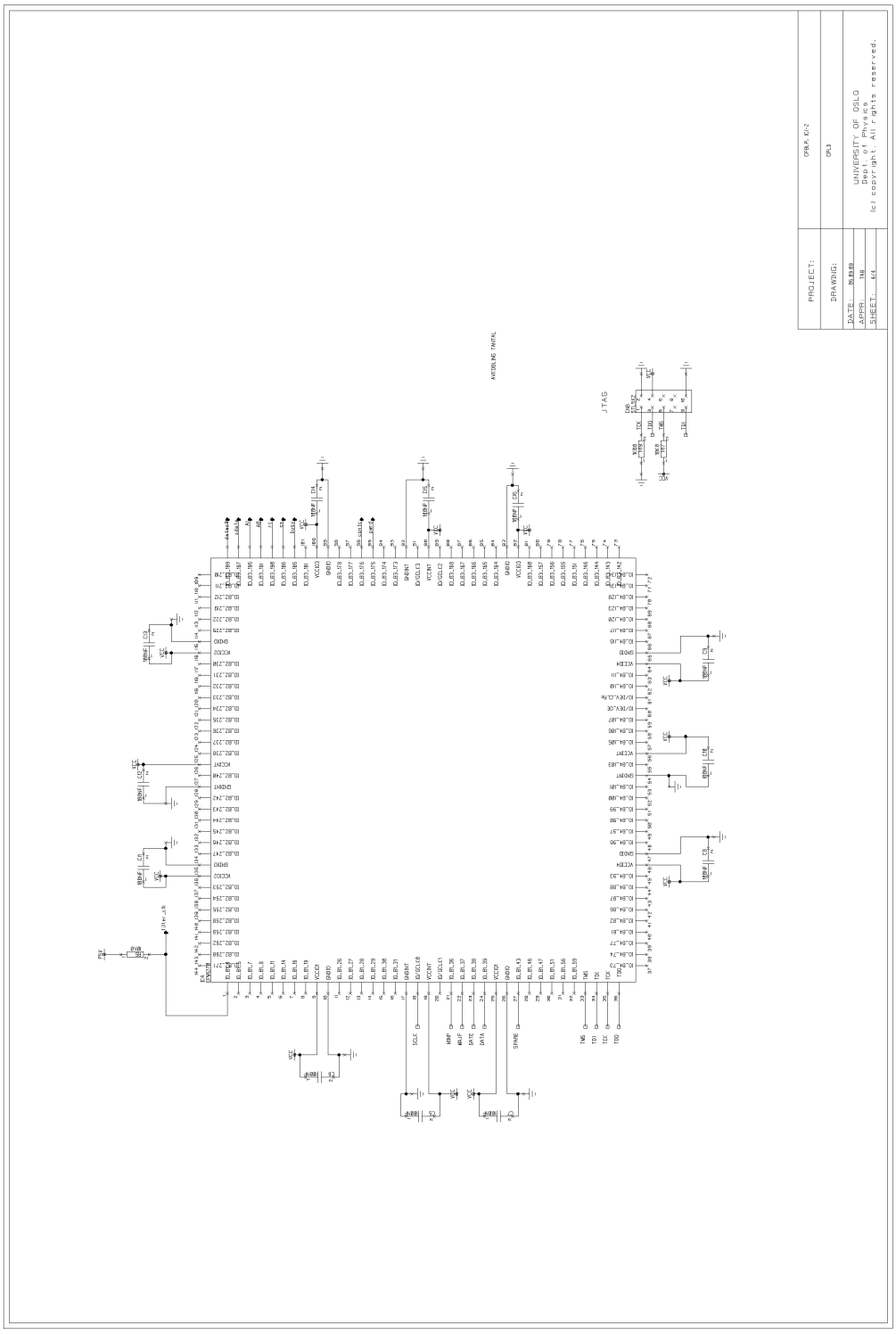


Figure A.4: DAQ card CPLD

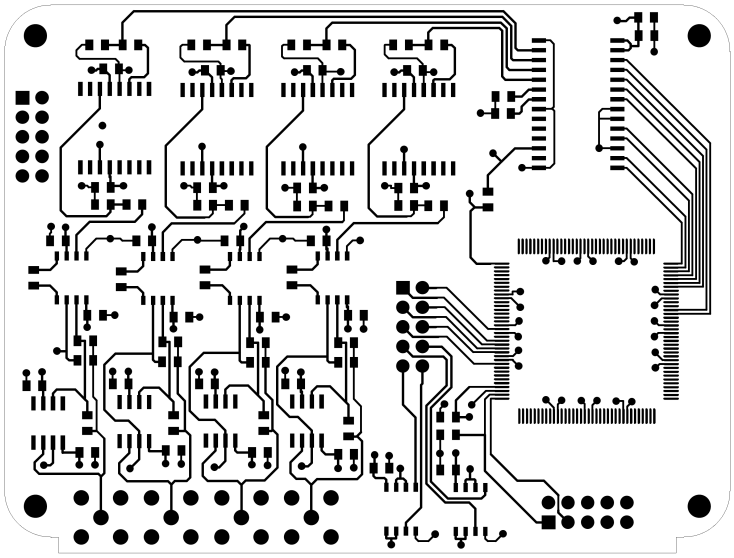


Figure A.5: DAQ card top electric PCB layout

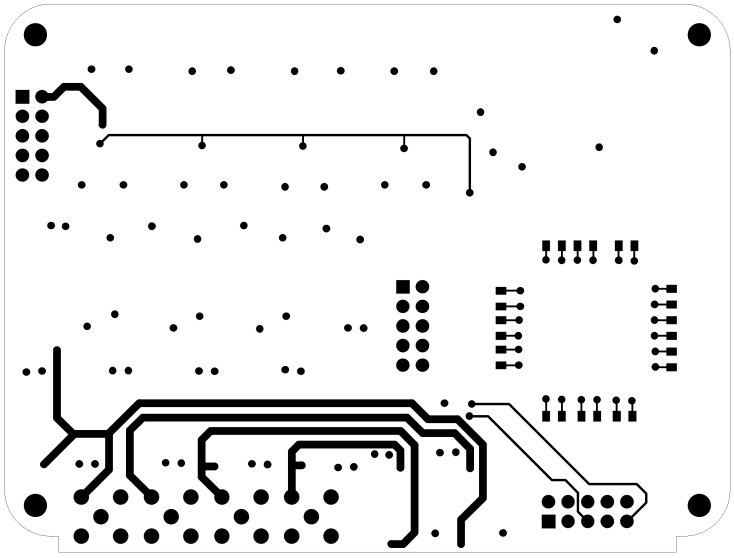


Figure A.6: DAQ card bottom electric PCB layout

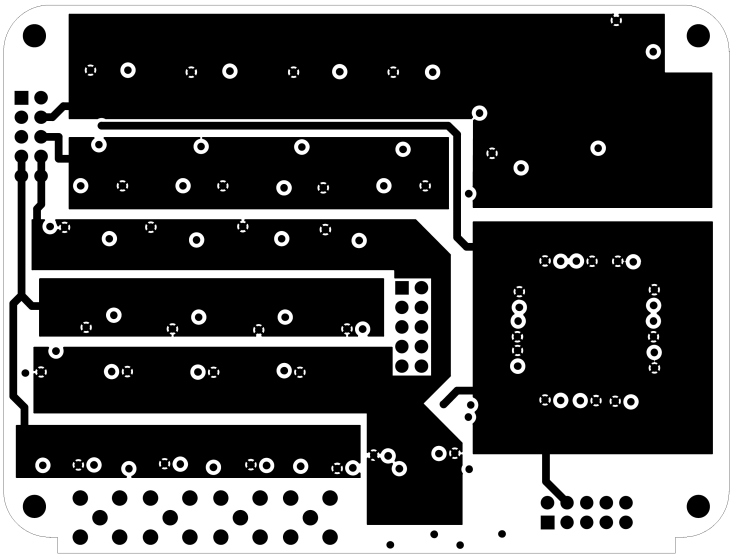


Figure A.7: DAQ card power plane PCB layout

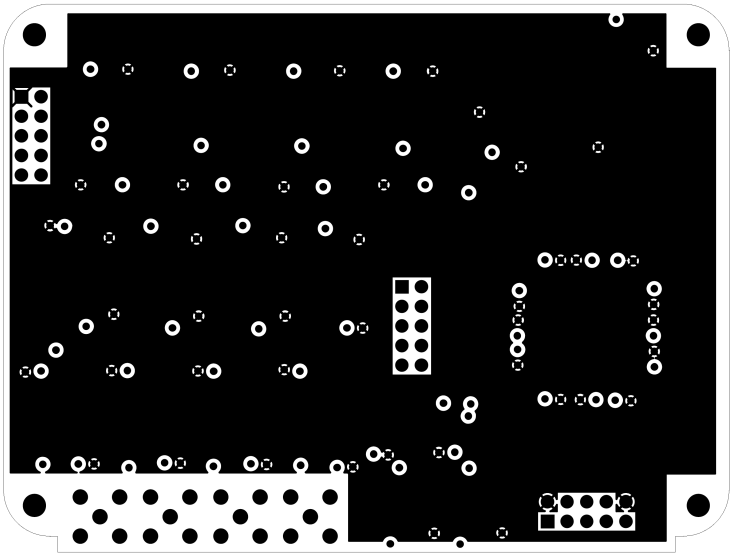


Figure A.8: DAQ card ground plane PCB layout

A.2 Power and Interface PCB

Listing: Parts list for Power/Interface board

Parts List

CADSTAR Design Editor Version 10.0.0.2

Part Name	Description	Qty.	Comps.
CAP/100NF/SMD0805R	10% 50V 0805 X7R	5	C1 C3–6
CON/DSUB15PF–HD	FEMALE 15 PINS HIGH DESITY	1	CN1
CON/STL5X2	5X2 SCOTT ELEC. PINROW	2	CN2–3
DIO/BAS16/SMD	DIODE SOT23	4	D1–4
MAXIM/MAX490/SMD	FULL DUPLEX TRANCIEVER	1	X2
OPTO/HCPL0631/SMD	HIGH SPEED OPTOCOUPLER	2	IC1–2
POW/78L05ACM/SMD	POS. VOLTAGE REGULATOR	1	X3
POW/79L05ACM/SMD	−5V REGULATOR	1	X5
POW/AD587/SMD	+10V REFERENCE	4	X10–13
POW/IMX4/DIP	DC–DC CON 4W VOUT +/− 5V	1	X1
POW/LM1117/SOT−223	+3.3V VOLTAGE REG.	1	X4
RES/10K0/SMD0805R	RESISTOR KOA 0805 1% 0.125W	4	R10–13
RES/8K20/SMD0805R	RESISTOR KOA 0805 1% 0.125W	5	R16
RES/120R/SMD0805R	RESISTOR KOA 0805 1% 0.125W	2	R8–9
RES/15K0/SMD0805R	RESISTOR KOA 0805 1% 0.125W	1	R15
RES/0R00/SMD0805R	RESISTOR KOA 0805 1% 0.125W	2	R1–2
RES/1K00/SMD0805R	RESISTOR KOA 0805 1% 0.125W	4	R4–7
RES/30K0/SMD0805R	RESISTOR KOA 0805 1% 0.125W	1	R14
RES/4K30/SMD0805R	RESISTOR KOA 0805 1% 0.125W	1	R18
RESNET/220R/SMD	RESISTOR ARRAY 1206	2	RNET1–2
SH3.0	HOLE FOR 3MM SCREW	4	SH1–4
TANT/10UF/16V/SMD	TANTAL ELECTROLYTIC CAP	1	C2
TANT/1UF/20V/SMD	TANTAL ELECTROLYTIC CAP	2	C7–8

End of report

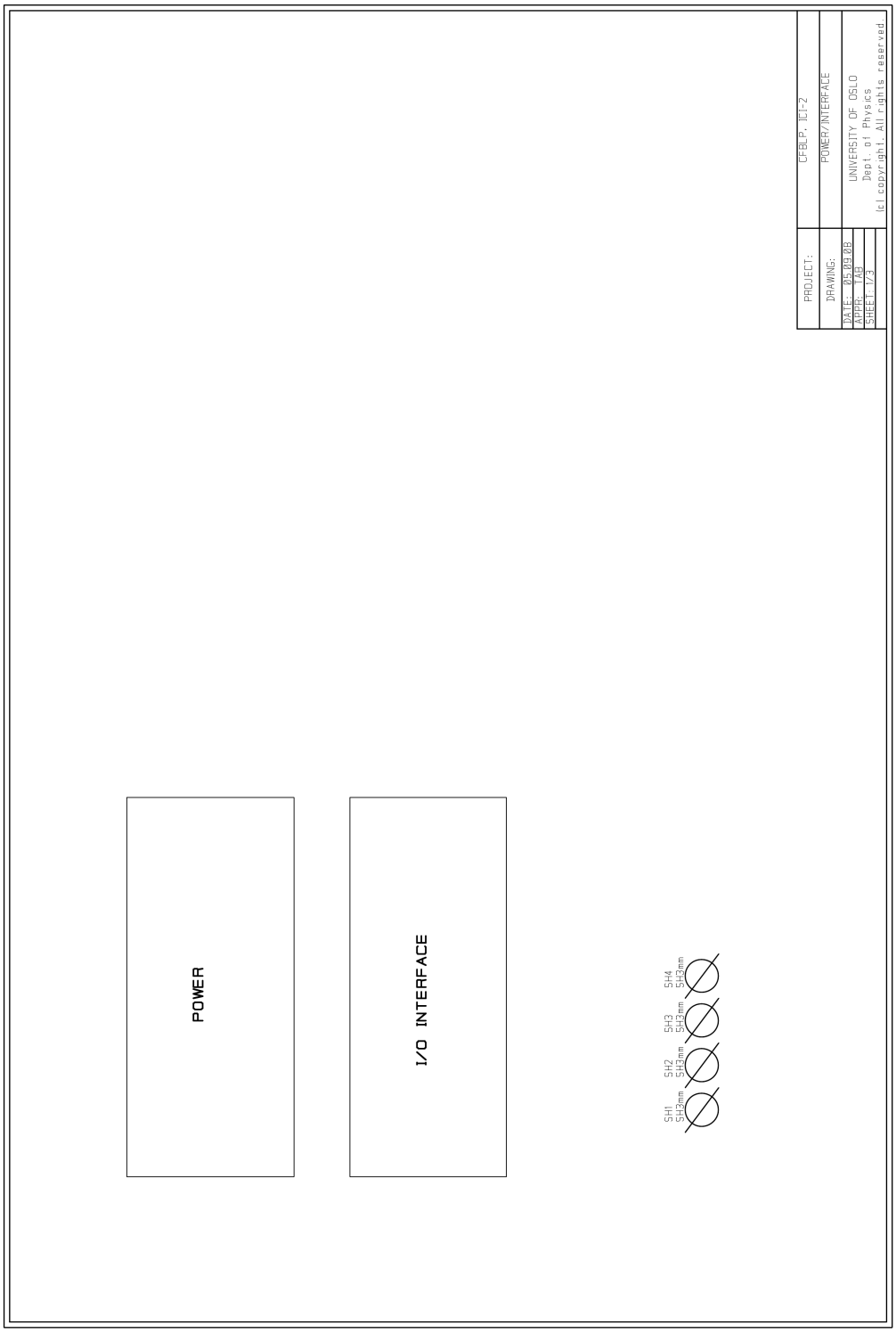


Figure A.9: Power/Interface card top schematics

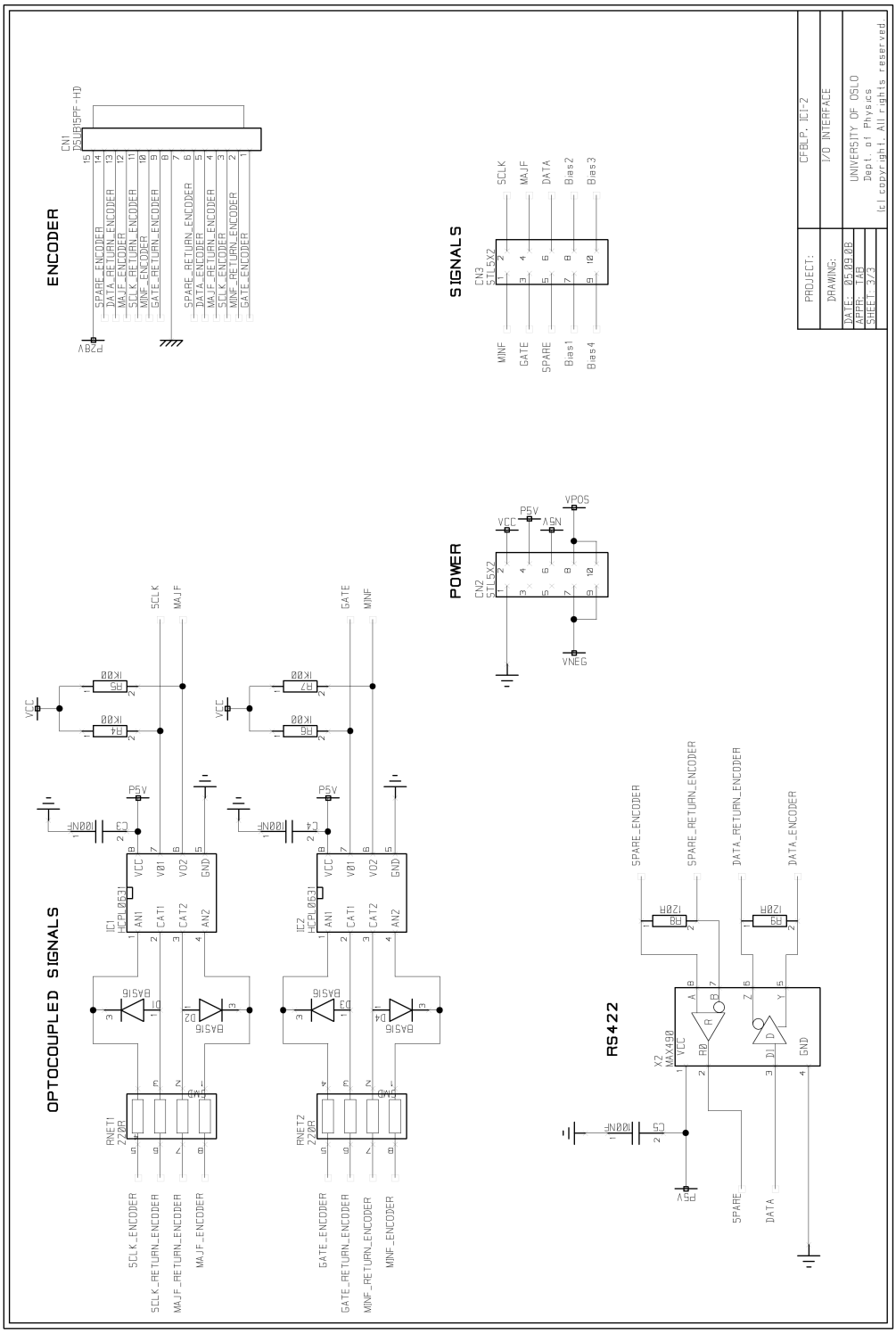


Figure A.10: Power/Interface card I/O interface

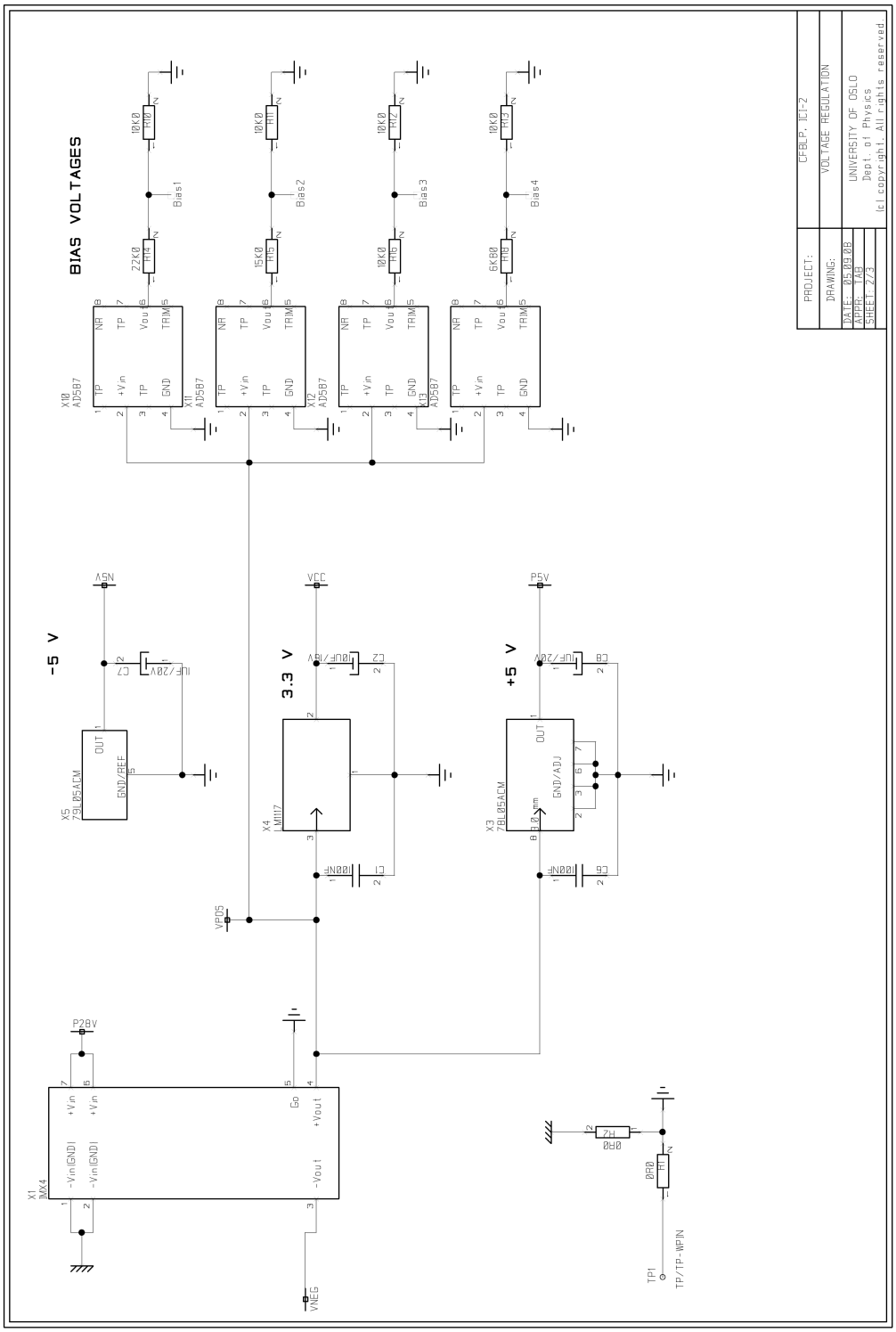


Figure A.11: Power/Interface card voltage regulation

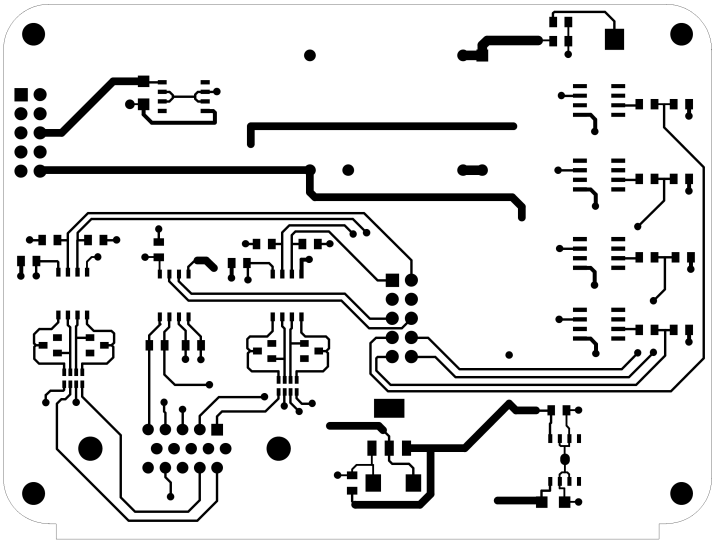


Figure A.12: Power/Interface card top electric PCB layout

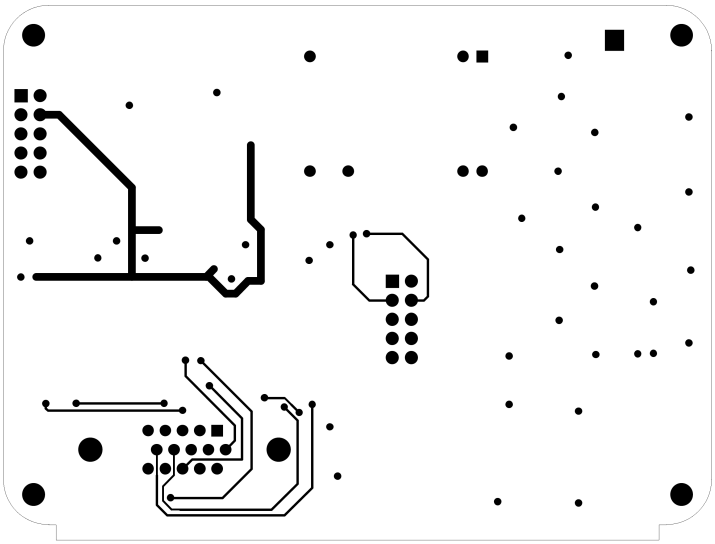


Figure A.13: Power/Interface card bottom electric PCB layout

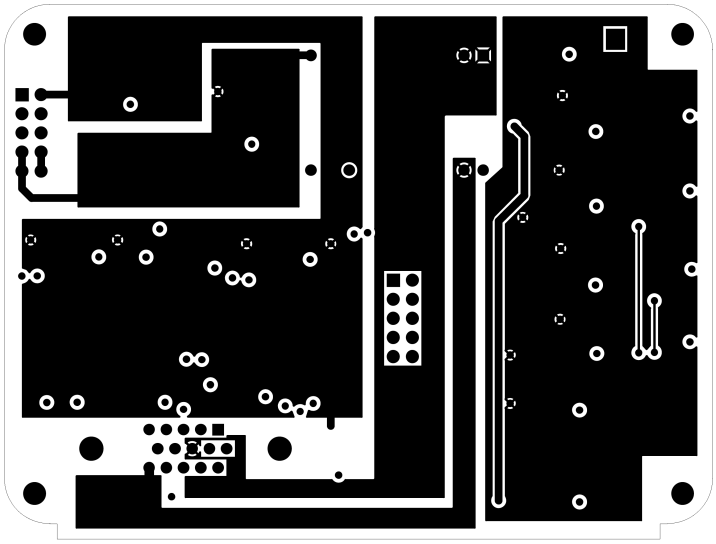


Figure A.14: Power/Interface card power plane PCB layout

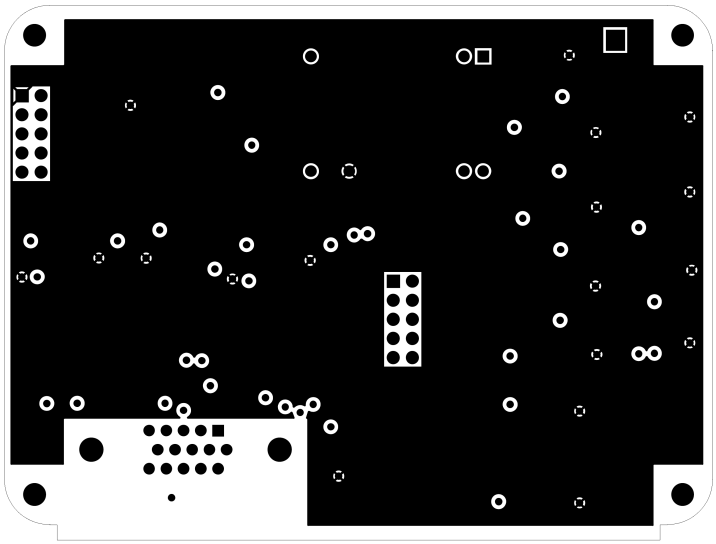


Figure A.15: Power/Interface card ground plane PCB layout

Appendix B

Data figures

This appendix contains the data figures from chapter 8 in larger format.

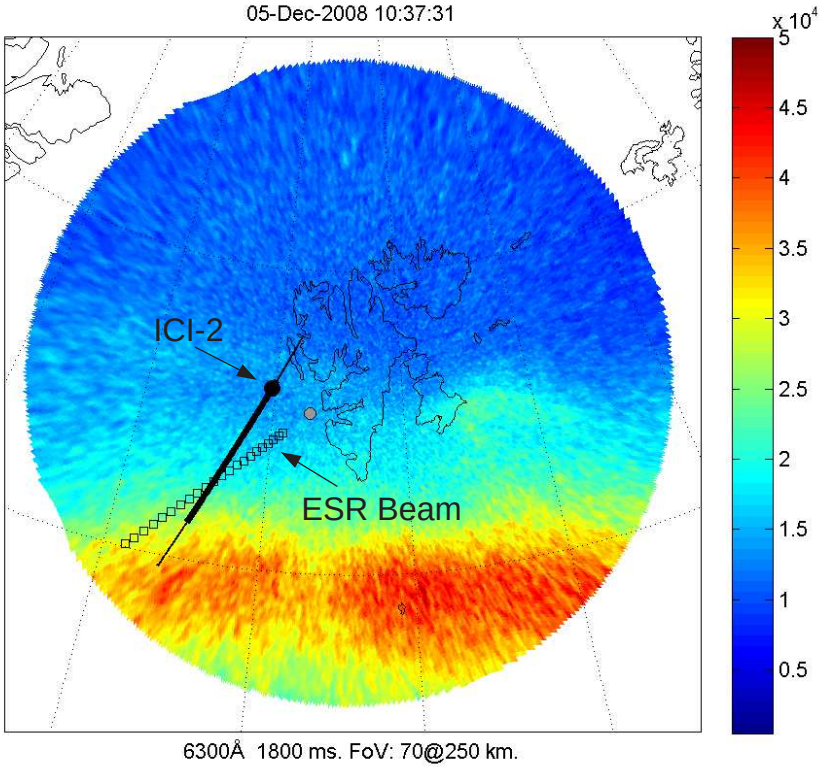


Figure B.1: Allsky camera

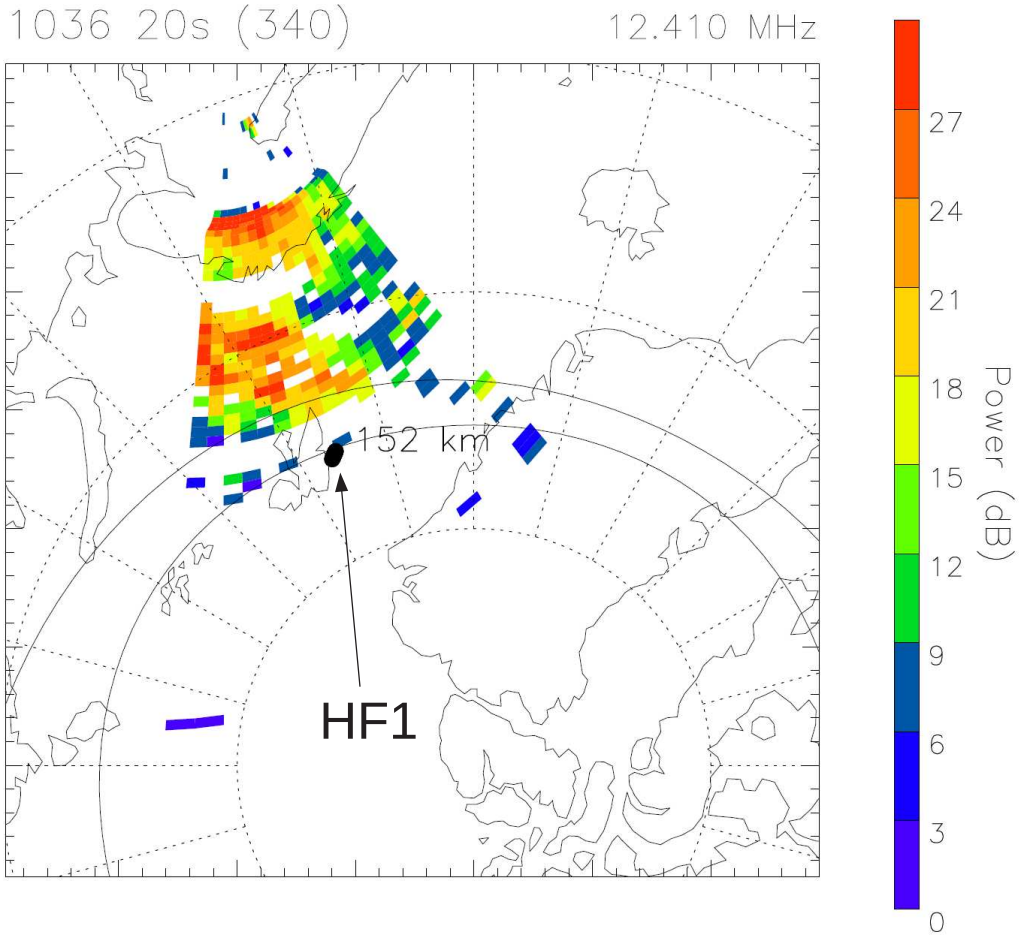


Figure B.2: Radar power density plot showing the rocket's first encounter with HF backscatter targets

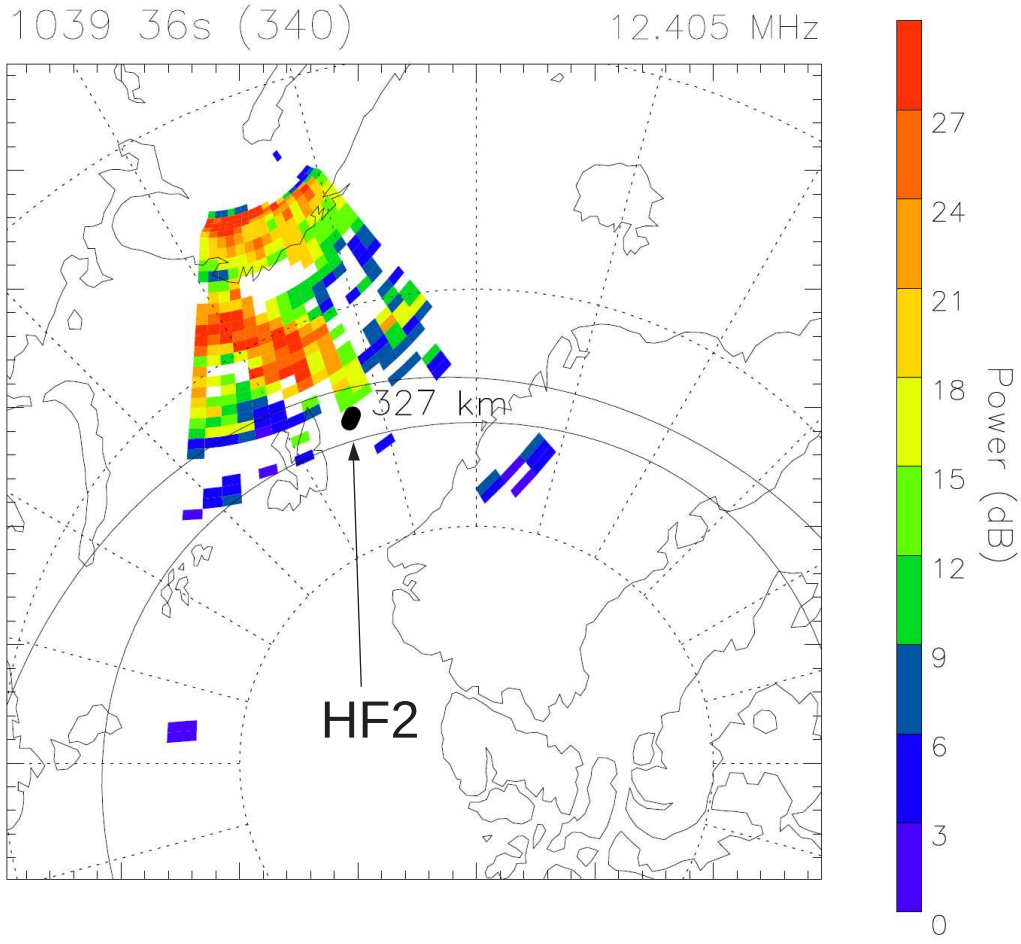


Figure B.3: Radar power density plot showing the rocket's second encounter with HF backscatter targets

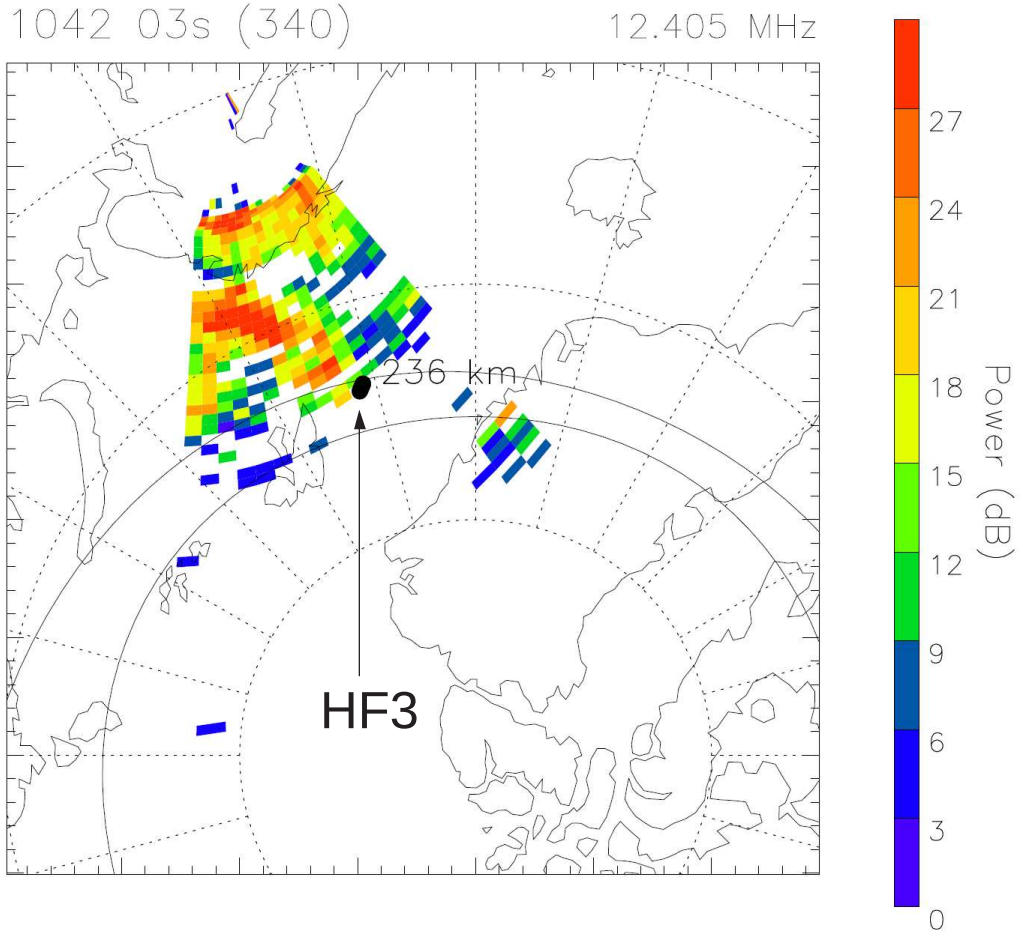


Figure B.4: Radar power density plot showing the rocket's third encounter with HF backscatter targets

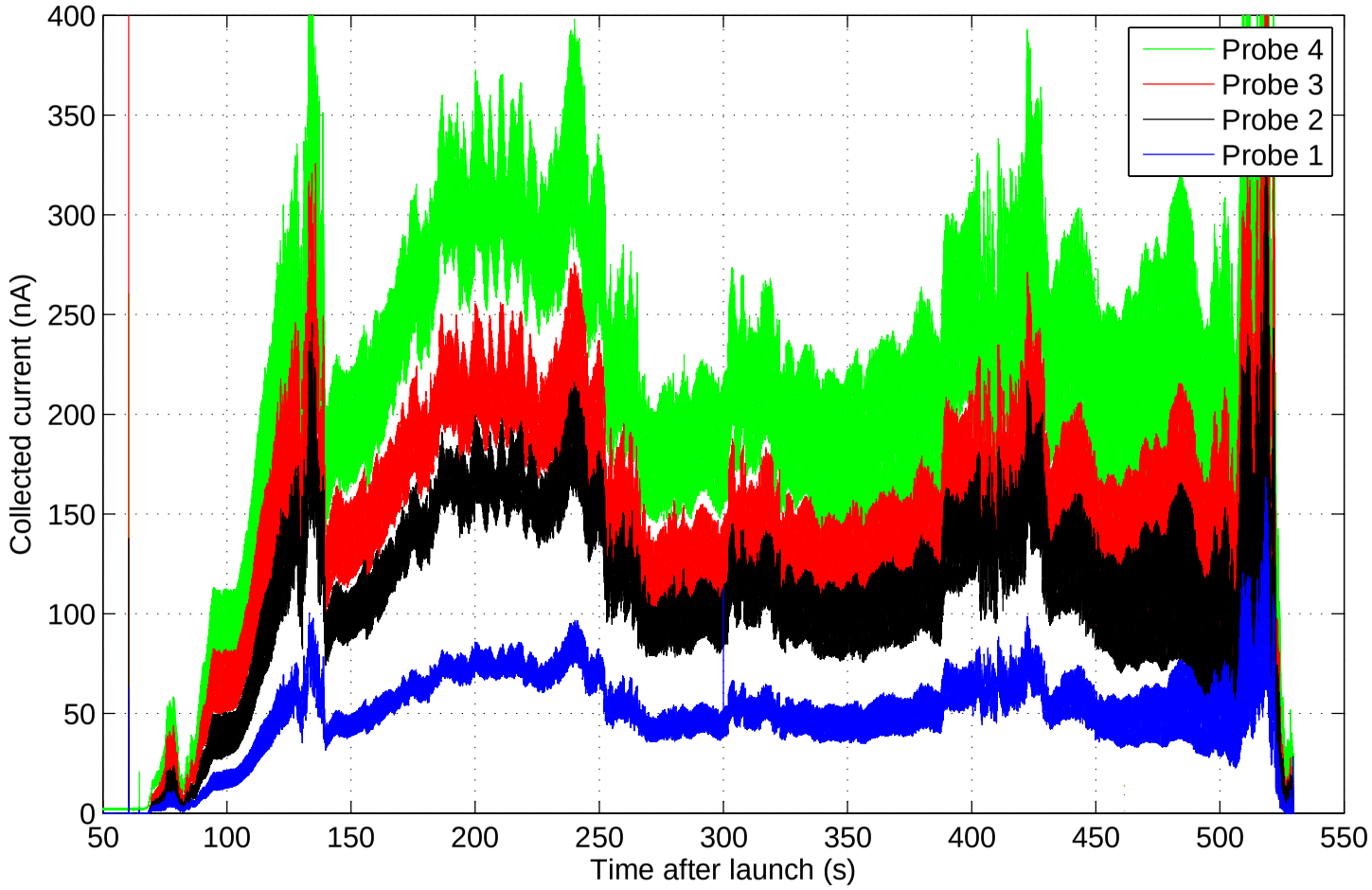


Figure B.5: Raw data from entire flight

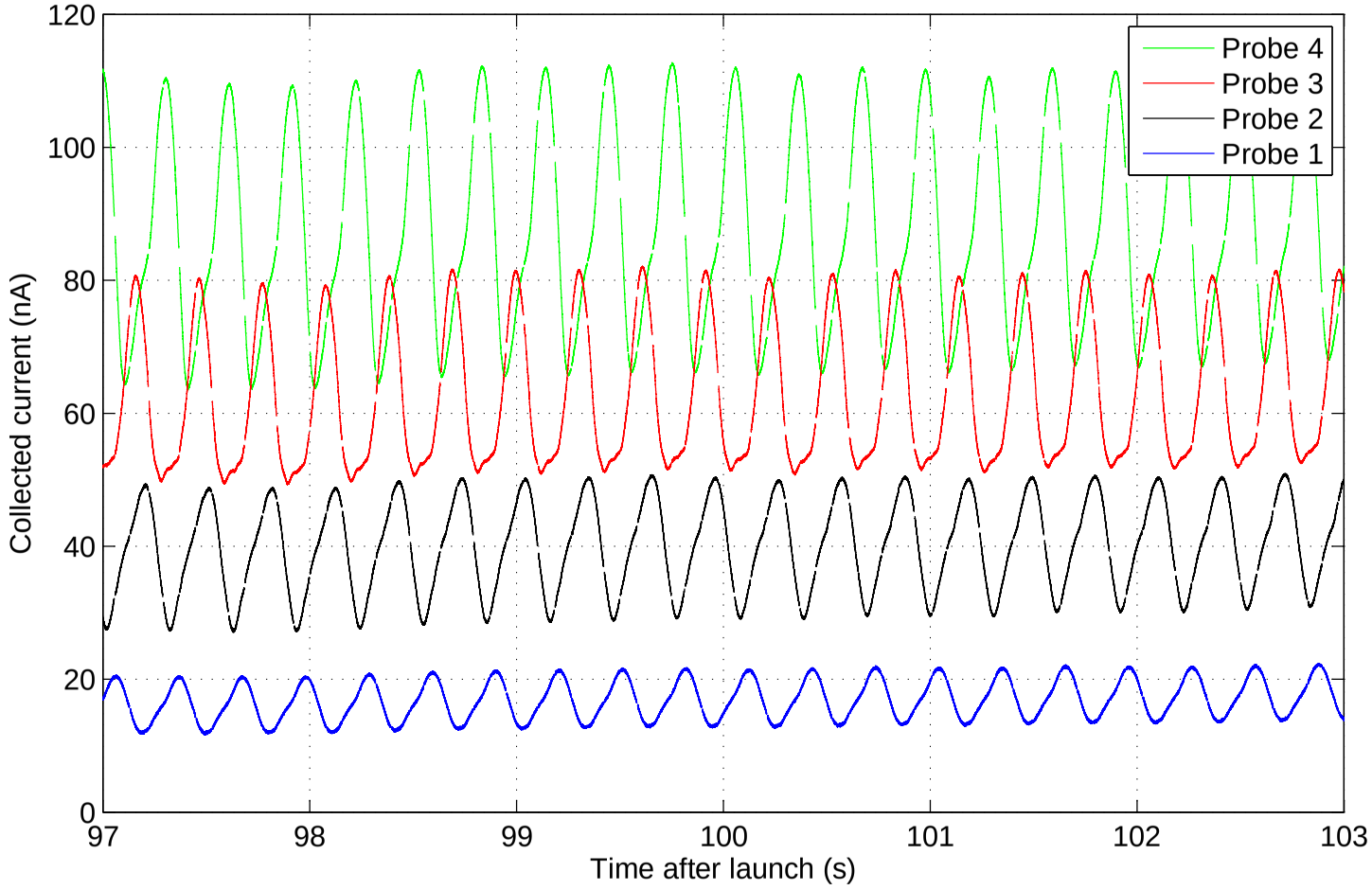


Figure B.6: Spin disturbance

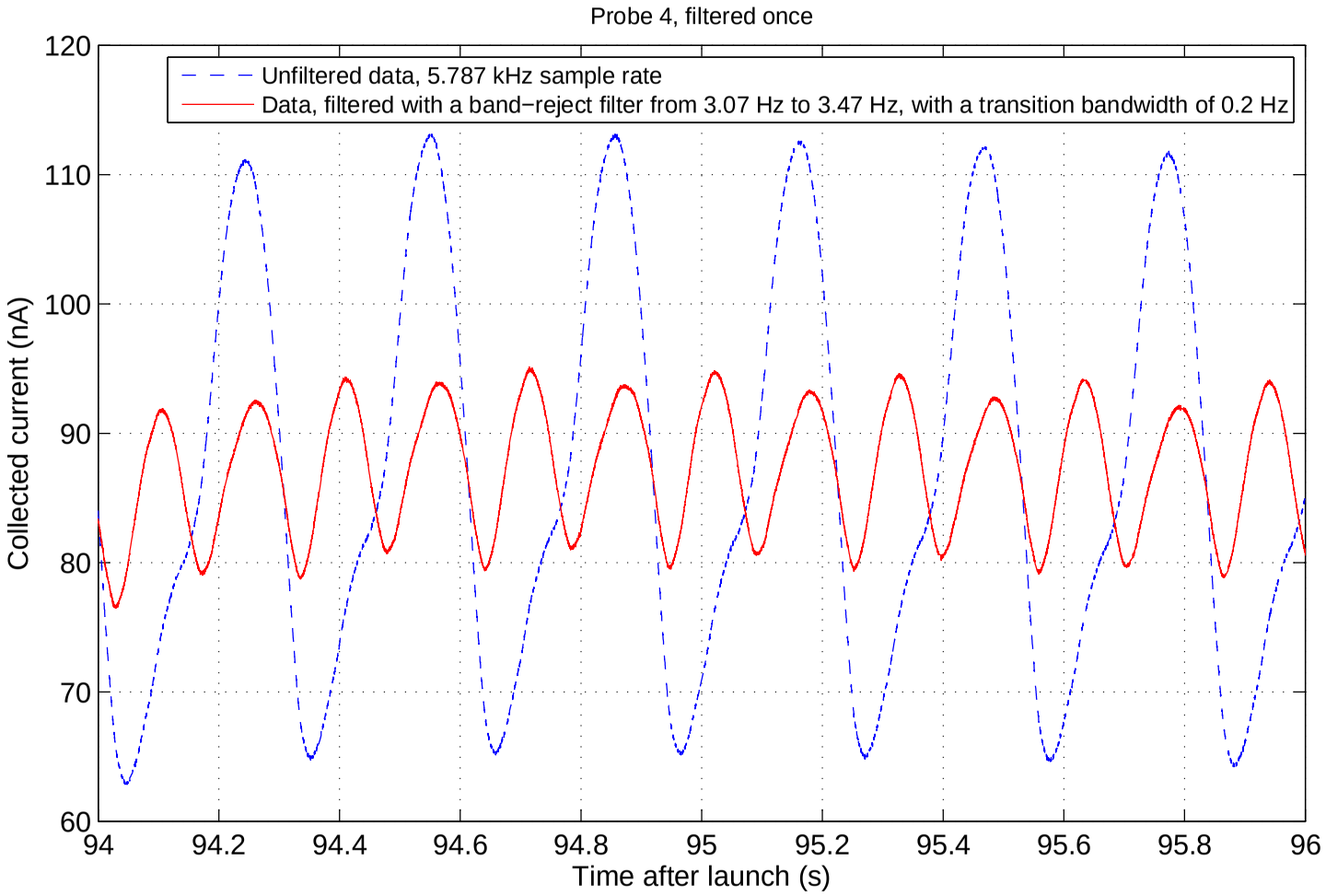


Figure B.7: Spin disturbance at 2x spinrate, due to boom geometry

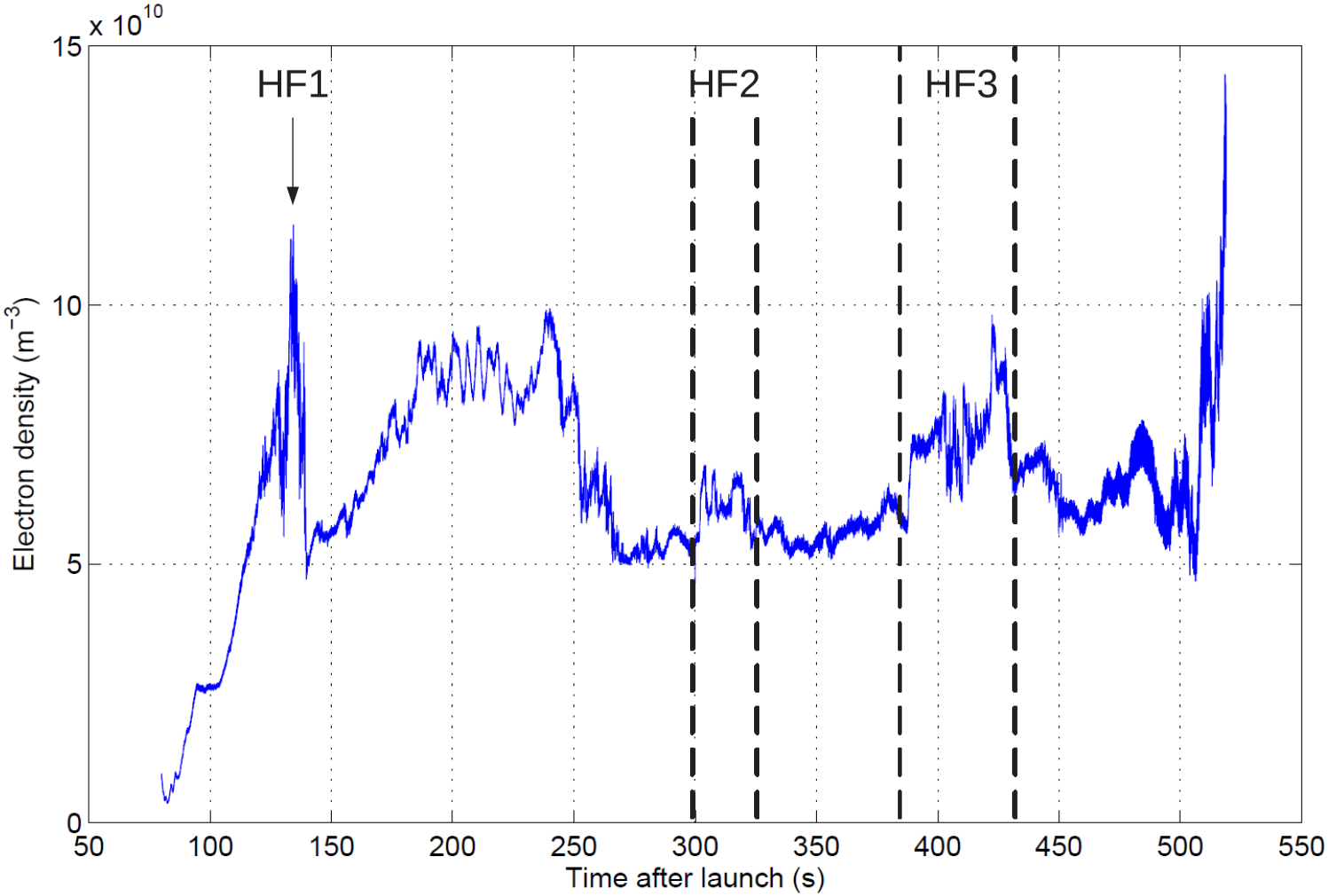


Figure B.8: Processed data from entire flight

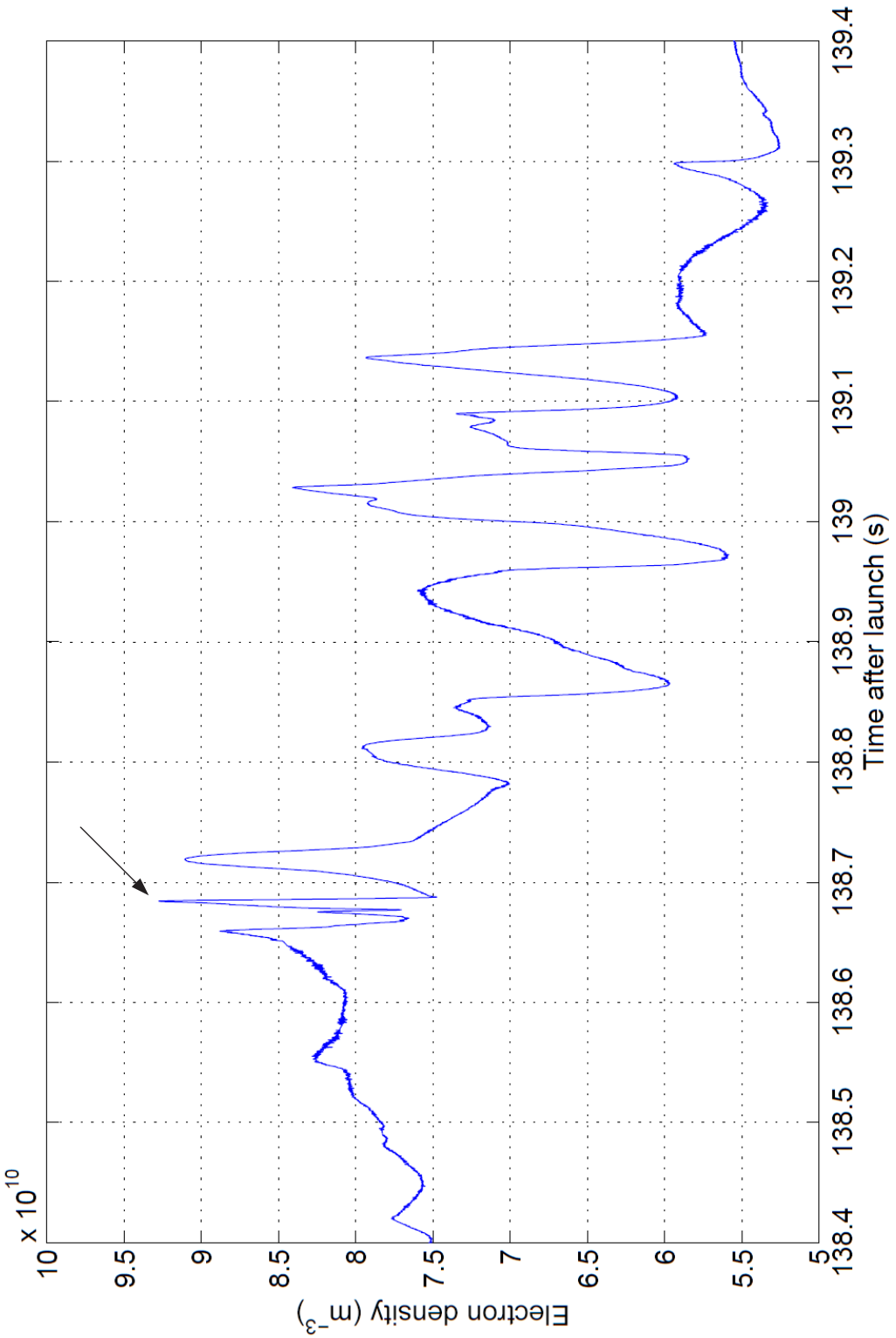


Figure B.9: Processed data showing fine structures down to about 15 meters in size (Between 138.6 and 138.7 second)

Appendix C

Program code

This appendix contains the code for Matlab calibration routines, and the VHDL code implemented in the CPLD.

C.1 Matlab code

Listing: Calibration coefficient routine

```
% Calibration routine for probe data, one channel
% "sorted2" is the extracted data for the measurement channel
% from the PCM encoder

midrange = 32263; % Measured midrange for the measurement channel
teller = 1000;
total = zeros(teller,1);
start=length(sorted2)-teller;
counting = 1;
lsb = 20/(2^16);

% for x=start:length(sorted2)
%     total(counting) = sorted2(x);
%     counting = counting + 1;
% end
% oneuAmean = mean(total)

Vmeas = zeros(counter2-30,1);
valid_points = length(Vmeas);

% Converts digital value to measured voltage on ADC,
% with adjustments for measured channel midrange
for x=1:valid_points
    %Vmeas(x) = (sorted2(x)-(2^15))*lsb;
    Vmeas(x) = (sorted2(x)-midrange)*lsb;
end

% Vector for the x-axis, with same length as measurement dataset
x_axis = linspace((-0.005*(10^-6)),(0.995*(10^-6)),length(Vmeas));

% Conversion from measured voltage to measured current
Imeas = -Vmeas/(4.7e6);
```

```
plot(x_axis,Imeas,'-k')
grid on
ylabel('Measured current (A)'), xlabel('Stimuli current (A)')
legend('Stepped current','Location','SouthEast')
title('Stimuli vs. output')
```

C.2 VHDL code

Listing: Top level VHDL file

```
-- Author        : Tore André Bekkeng
-- Company       : University of Oslo
-- File name     : CFBLP_v1_ICI2.vhd
-- Date          : 31.08.2008
-- Version       : 1
-- Project       : ICI-2
-- Function      : Data acquisition for CFBLP v1


library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

use work.comp_package.all;                -- User defined components

entity CFBLP_v1_ICI2 is

  port
    (
        not_sclk     : in     std_logic;
        not_gate     : in     std_logic;
        not_minf     : in     std_logic;
        busy         : in     std_logic;
        sdata        : in     std_logic;
        data         : out    std_logic;
        dataclk      : out    std_logic;
        cs           : out    std_logic;
        rc           : out    std_logic;
        CH_select    : out    std_logic_vector(1 downto 0);
        pwrd         : out    std_logic;
        contc        : out    std_logic;
        filter_clk   : out    std_logic;
        not_majf     : in     std_logic;
        not_spare    : in     std_logic
    );

end CFBLP_v1_ICI2;

architecture CFBLP_v1_ICI2_arch of CFBLP_v1_ICI2 is


-------------------------------------------------------------------------------
--                          COMPONENT DECLARATIONS
-------------------------------------------------------------------------------


component ADS7825 is
  port
    (
        adc_clk      : in           std_logic;                  -- System clock
        start_conv   : in           std_logic;                  -- Sync to TM-format
        sdata        : in           std_logic;                  -- Serial data from ADC
        busy         : in           std_logic;
        cs           : out          std_logic;
        rc           : out          std_logic;
        pwrd         : out          std_logic;
```

```
        contc       : out           std_logic;
        dataclk     : out           std_logic;                          -- Clock to converter
        ch_select   : out           std_logic_vector(1 downto 0);  -- ch. sel. bits A1 /A0
        Pdata_CH0   : out           std_logic_vector(15 downto 0); -- to encoder
        Pdata_CH1   : out           std_logic_vector(15 downto 0); -- to encoder
        Pdata_CH2   : out           std_logic_vector(15 downto 0); -- to encoder
        Pdata_CH3   : out           std_logic_vector(15 downto 0); -- to encoder
        DataReady   : out           std_logic                           -- All channels
    );

end component;

component clock18div is
        port
        (
        clk_in  : in  std_logic;
    reset   : in  std_logic;
    clk_out : out std_logic
        );

end component;
```

```
-------------------------------------------------------------------------------
--                          SIGNALS
-------------------------------------------------------------------------------

-- Signals from TM encoder
signal sclk             : std_logic;
signal minf             : std_logic;
signal gate             : std_logic;
signal majf             : std_logic;
signal spare            : std_logic;

-- Signals from ADC
signal Pdata_CH0        : std_logic_vector(15 downto 0);
signal Pdata_CH1        : std_logic_vector(15 downto 0);
signal Pdata_CH2        : std_logic_vector(15 downto 0);
signal Pdata_CH3        : std_logic_vector(15 downto 0);
signal Pdata_Ready      : std_logic;
signal dataclk_temp     : std_logic;
signal test_cnt         : std_logic_vector(15 downto 0);

-- Internal reset signals
signal reset            : std_logic;
signal reset_sync       : std_logic;    -- Synchronize to TM-encoder
signal reset_sync_majf  : std_logic;    -- Synchronize to TM-encoder

-- Internal TM counters
signal bit_cnt          : std_logic_vector(2 downto 0);
signal WordStrobe       : std_logic;
signal word_cnt         : std_logic_vector(7 downto 0);
signal frame_cnt        : std_logic_vector(1 downto 0);

signal gate_delayed     : std_logic;                        -- To not loose MSB in TM
signal DataSample       : std_logic_vector(15 downto 0);  -- Data to TM Shift reg.
signal load_sample      : std_logic;
signal load_sample_del  : std_logic;                        -- Enable/disable TM shift reg

-- Internal signals
```

```
signal conv              : std_logic;
signal adc_clock         : std_logic;
signal filter_clock      : std_logic;

-- Stored data values
signal data_CH0          : std_logic_vector(15 downto 0);  -- Stored data for ADC CH0
signal data_CH1          : std_logic_vector(15 downto 0);  -- Stored data for ADC CH1
signal data_CH2          : std_logic_vector(15 downto 0);  -- Stored data for ADC CH2
signal data_CH3          : std_logic_vector(15 downto 0);  -- Stored data for ADC CH3
signal data_ready        : std_logic;                      -- High when data ready


-- Type definitions
type statetype1 is (SyncCheck, IgnoreSt);
signal sync_state : statetype1;

type statetype2 is (SyncCheck_majf, IgnoreSt_majf);
signal sync_state_majf : statetype2;


begin

-------------------------------------------------------------------------------
--                          PORT MAPPING
-------------------------------------------------------------------------------




-- Data transfer shift register
Com_SR: SR_par2ser_redge
generic map (16)
port map (sclk, DataSample, load_sample_del, gate_delayed, reset, data);

-- 4 - Channel ADC
ADC : ADS7825
port map (adc_clock, conv, sdata, busy, cs, rc, pwrd, contc, dataclk_temp,
                  CH_select, Pdata_CH0, Pdata_CH1, Pdata_CH2, Pdata_CH3, data_Ready);

--Clock divider (18)
Clk_Div: clock18div
port map(sclk, reset, filter_clock);

-------------------------------------------------------------------------------



-- Invert again the signals inverted in the optocouplers
sclk <= not(not_sclk);
minf <= not(not_minf);
majf <= not(not_majf);
spare <= not(not_spare);
gate <= not(not_gate);

-- Signal throughput
filter_clk <= filter_clock;
dataclk <= dataclk_temp;
adc_clock <= sclk;

reset <= '0';
```

```
-------------------------------------------------------------------------------
--                          WORD STROBE
-------------------------------------------------------------------------------

BITCOUNTER:
process(sclk, reset_sync)
begin
  if reset_sync = '1' then              -- asyncron
    bit_cnt <= (others => '0');
  elsif falling_edge(sclk) then
    bit_cnt <= bit_cnt + 1;
  end if;
end process;


WORDSYNC:
process(sclk)
begin
  if rising_edge(sclk) then
    if (bit_cnt = 7) then
      WordStrobe <= '1';
    else
      WordStrobe <= '0';
    end if;

  end if;
end process;


-------------------------------------------------------------------------------
--                          WORD COUNTER
-------------------------------------------------------------------------------

-- 144 words per frame

WORDCOUNTER:
process(sclk, reset_sync)
begin
  if (reset_sync = '1') then
    word_cnt <= (others => '0');
  elsif falling_edge(sclk) then
    if (WordStrobe = '1') then
      if (word_cnt < 143) then
        word_cnt <= word_cnt + 1;
      else
        word_cnt <= (others => '0');
      end if;
    end if;
  end if;
end process;



-------------------------------------------------------------------------------
--                          FRAMECOUNTER
-------------------------------------------------------------------------------

FRAMECOUNTER:
process(sclk, reset_sync_majf)
begin
  if (reset_sync_majf = '1') then
```

```
    frame_cnt <= (others => '0');
  elsif rising_edge(sclk) then
    if (word_cnt = 143 and bit_cnt = 0) then
      frame_cnt <= frame_cnt + 1;
    end if;
  end if;
end process;
```

-- FSM SYNCRONIZERS

```
-- Synchronize / reset bit & word counter to minf from PCM encoder
FSM_MINF_MAJF_SYNC:
process(sclk)
begin
  if rising_edge(sclk) then
    case sync_state is
      when SyncCheck =>
        --if (minf = '1' or majf = '1') then  "majf not in use"
        if (minf = '1') then
          reset_sync <= '1';
          sync_state <= IgnoreSt;
        else
          reset_sync <= '0';
          sync_state <= SyncCheck;
        end if;

       when IgnoreSt =>
        reset_sync <= '0';
                        --if (minf = '0' and majf = '0') then  "majf not in use"
        if (minf = '0') then
           sync_state <= SyncCheck;
         else
           sync_state <= IgnoreSt;
         end if;
    end case;
  end if;
end process;

reset_sync_majf <= '0';                    -- majf not in use
```

-- GATE DELAY

```
-- Delay of the gate signal, to avoid losing msb

GATEDELAY:
process(sclk)
begin
  if rising_edge(sclk) then
    if(gate = '1') then
      gate_delayed <= '1';
    else
      gate_delayed <= '0';
    end if;
  end  if;
end  process;
```

```
-------------------------------------------------------------------------------
--                          ADC CONVERSION CONTROL
-------------------------------------------------------------------------------
-- Control af ADS7825 4-channel 16-bit ADC

ADC_CONVERSION:
process(adc_clock)
begin
  if rising_edge(adc_clock) then
    if (word_cnt = 35 or word_cnt = 107) then
      conv <= '1';
    else
      conv <= '0';
    end if;
  end if;
end  process;


-------------------------------------------------------------------------------
--                          DATA HANDLING / STORAGE
-------------------------------------------------------------------------------
DATA_SHIFTING:
process(sclk)
begin
        if rising_edge(sclk) then
                if (data_ready = '1') then
                data_CH0 <= Pdata_CH0;
                data_CH1 <= Pdata_CH1;
                data_CH2 <= Pdata_CH2;
                data_CH3 <= Pdata_CH3;
                end if;
        end if;
end process;


-------------------------------------------------------------------------------
--                          DATA COMMUNICATION WITH ENCODER
-------------------------------------------------------------------------------


-- load data into the SR in the word before transfer
-- First transmission of data in current minf is from last conversion in previous minf
DATA_TRANSFER:
process(sclk)
begin
  if rising_edge(sclk) then

      load_sample <= '0';

      -- CH0
      if ((word_cnt = 35 or word_cnt = 107) and bit_cnt = 0) then
--                test_cnt <= test_cnt+1;
--                DataSample  <= test_cnt;
--          load_sample <= '1';
        DataSample  <= data_CH0;
        load_sample <= '1';

      -- CH1
```

```
      elsif ((word_cnt = 43 or word_cnt = 115) and bit_cnt = 0) then
--                test_cnt <= test_cnt+1;
--                DataSample  <= test_cnt;
--          load_sample <= '1';
        DataSample  <= data_CH1;
        load_sample <= '1';

      -- CH2
      elsif ((word_cnt = 51 or word_cnt = 123) and bit_cnt = 0) then
--                test_cnt <= test_cnt+1;
--                DataSample  <= test_cnt;
--          load_sample <= '1';
        DataSample <= data_CH2;
        load_sample <= '1';

      -- CH3
      elsif ((word_cnt = 59 or word_cnt = 131) and bit_cnt = 0) then
--                test_cnt <= test_cnt+1;
--                DataSample  <= test_cnt;
--          load_sample <= '1';
        DataSample <= data_CH3;
        load_sample <= '1';

      end if;
    end if;
  end process;




  -- Delay the load signal to SR with one half clock periode,
  -- because data are transmitted from the shift register on the
  -- rising edge, the same flank as the data transfer process uses.
  LOAD_DELAY:
  process(sclk)
  begin
    if falling_edge(sclk) then
      if (load_sample = '1') then
        load_sample_del <= '1';
      else
        load_sample_del <= '0';
      end if;
    end if;
  end process;


end CFBLP_v1_ICI2_arch;
```

Listing: ADC control

```
-- Author        : Tore André Bekkeng
-- Company       : University of Oslo
-- File name     : ADS7825.vhd
-- Date          : 31.08.08
-- Version       : 01
-- Project       : ICI-2
-- Function      : Controls the 4-channel ADC ADS7825


library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;


use work.comp_package.all;

entity ADS7825 is

  port
    (
        adc_clk     : in          std_logic;                      -- System clock
        start_conv  : in          std_logic;                      -- Sync to TM-format
        sdata       : in          std_logic;                      -- Serial data from ADC
        busy        : in          std_logic;
        cs          : out         std_logic;
        rc          : out         std_logic;
        pwrd        : out         std_logic;
        contc       : out         std_logic;
        dataclk     : out         std_logic;                      -- Clock to converter
        ch_select   : buffer      std_logic_vector(1 downto 0);   -- ch. sel. bits A1/A0
        Pdata_CH0   : buffer      std_logic_vector(15 downto 0);  -- to encoder
        Pdata_CH1   : buffer      std_logic_vector(15 downto 0);  -- to encoder
        Pdata_CH2   : buffer      std_logic_vector(15 downto 0);  -- to encoder
        Pdata_CH3   : buffer      std_logic_vector(15 downto 0);  -- to encoder
        DataReady   : buffer      std_logic                       -- All channels
    );


end ADS7825;


architecture ADS7825_arch of ADS7825 is


-------------------------------------------------------------------------------
--                          COMPONENT DECLARATIONS
-------------------------------------------------------------------------------
 component SR_SerIn_redge is
    port
    (
    clk       : in  std_logic;
    DataIn    : in  std_logic;
    shift_en  : in  std_logic;
    DataOut   : out std_logic_vector(15 downto 0)
    );
end component;

-------------------------------------------------------------------------------
--                          CONSTANTS
```

```
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
--                          SIGNALS
-----------------------------------------------------------------------------

signal conv             : std_logic;
signal reset            : std_logic;
signal Dcnt             : std_logic_vector(3 downto 0);
signal Pdata            : std_logic_vector(15 downto 0);
signal sr_enable        : std_logic;

--typedef.
type statetype is (PowerUp, Check_conv, Enable_ADC, Start_conversion,
                                        Conversion_started, Check_busy, Finconversion,
                                        Prepare_read, Wait1, Enable_sr, Read_sdata,
                                        Finread, MSB_conv);

signal state : statetype;



begin
 reset <= '0';
 dataclk <= adc_clk; -- Throuthput av sclk
--clk    <= sclk;

-----------------------------------------------------------------------------
--                          PORT MAPPING & GENERIC MAPPING
-----------------------------------------------------------------------------

SR_DATA: SR_SerIn_redge

  port map (adc_clk, sdata, sr_enable, Pdata );



-----------------------------------------------------------------------------
--                          CONVERSION CONTROL
-----------------------------------------------------------------------------


-- Conversion synchronized to TM-format
-- Uses the components "start_conv" input.

conv <=  start_conv;


-----------------------------------------------------------------------------
--                          FSM CONF / READ
-----------------------------------------------------------------------------
-- Read the channels in the following  order: 0,1,2,3

FSM_CONF_READ:
process(adc_clk, reset)
```

```
begin
  if (reset = '1') then
    state <= PowerUp;
  elsif rising_edge(adc_clk) then

    -- set default values
    cs        <= '1';
        rc        <= '0';
    sr_enable <= '0';
    DataReady <= '0';
        contc     <= '0';
        pwrd      <= '0';


      case state is
    when PowerUp =>
      state <= Check_conv;

    when Check_conv =>
              rc <= '1';
              CH_select <= "11"; --Due to conversion result from CH_select n + 1
              if (conv = '1') then
                      state <= Enable_ADC;
              else
                      state <= Check_conv;
              end if;

        when Enable_ADC =>
              cs <= '0';
              rc <= '1';
              state <= Start_conversion;

        when Start_conversion =>
              rc <= '0';
              cs <= '0';
              state <= Conversion_started;

        when Conversion_started =>
              cs <= '1';
              rc <= '0';
              state <= Check_busy;

        when Check_busy =>
              rc <= '0';
              if (busy = '1') then
                      state <= Finconversion;
              else
                      state <= Check_busy;
              end if;

        when Finconversion =>
              rc <= '1';
              state <= Prepare_read;

        when Prepare_read =>
              cs <= '0';
              rc <= '1';
              state <= Wait1;

        when Wait1 =>
              rc <= '1';
              cs <= '0';
```

```
                state <= Enable_sr;

            when Enable_sr =>
                sr_enable <= '1';
                rc <= '1';
                cs <= '0';
                state <= Read_sdata;

            when Read_sdata =>
                cs <= '0';
                rc <= '1';
                if (Dcnt = 15) then
                        sr_enable <= '0';
                        state <= Finread;
                        Dcnt <= "0000";
                else
                        Dcnt <= Dcnt + 1;
                        sr_enable <= '1';
                        state <= Read_sdata;
                end if;

        when  FinRead =>
          if (CH_select = "11") then
            Pdata_CH0 <= Pdata;
            CH_select <= CH_select + 1;
                    rc <= '1';
                    cs <= '0';
            state <= Enable_ADC;
          elsif (CH_select = "00") then
            Pdata_CH1 <= Pdata;
            CH_select <= CH_select + 1;
                    rc <= '1';
                    cs <= '0';
            state <= Enable_ADC;
                    elsif (CH_select = "01") then
                      Pdata_CH2 <= Pdata;
                      CH_select <= CH_select + 1;
                      rc <= '1';
                      cs <= '0';
                      state <= Enable_ADC;
          elsif (CH_select = "10") then
            Pdata_CH3 <= Pdata;
--            DataReady <= '1';
--                    rc <= '1';
--                    cs <= '0';
            state <= MSB_conv;
          else
            state <= PowerUp;
          end if;

            when MSB_conv =>
                    Pdata_CH0(15) <= not(Pdata_CH0(15));
                    Pdata_CH1(15) <= not(Pdata_CH1(15));
                    Pdata_CH2(15) <= not(Pdata_CH2(15));
                    Pdata_CH3(15) <= not(Pdata_CH3(15));
          DataReady <= '1';
                    rc <= '1';
                    cs <= '0';
                    state <= Check_conv;


        when others =>
```

```
        state <= PowerUp;                -- Fault tolerance

    end case;

  end if;
end  process FSM_CONF_READ;



end ADS7825_arch;
```

Listing: Shift register, serial in, parallel out

```
-- Author        : Tore André Bekkeng
-- Company       : University of Oslo
-- File name     : SR_SerIn_redge.vhd
-- Date          : 23.04.08
-- Version       : 01
-- Project       : ICI-2
-- Function      : Serial skift register, rising edge.



library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity SR_SerIn_redge is
  generic (
    width : integer := 16);


  port
    (
    clk       : in  std_logic;
    DataIn    : in  std_logic;
    shift_en  : in  std_logic;
    DataOut   : out std_logic_vector(width-1 downto 0)
    );

end SR_SerIn_redge;


architecture SR_SerIn_arch of SR_SerIn_redge is

  signal data_int : std_logic_vector(width-1 downto 0);


begin

  SHIFT_REG:
  process (clk)
  begin

   if rising_edge(clk) then
      if (shift_en = '1') then
        data_int(0) <= DataIn;
        for i in width-2 downto 0 loop
          data_int(i+1) <= data_int(i);
        end loop;
      end if;

    end if;
  end process SHIFT_REG;

  DataOut <= data_int;



end SR_SerIn_arch;
```

Listing: Shift register, parallel in, serial out

```
-- Author        :  Tore André Bekkeng
-- Company       : University of Oslo
-- File name     : SR_par2ser_redge.vhd
-- Date          : 23.04.08
-- Version       : 02
-- Project       : ICI-2
-- Function      : Paralell to serial skift register, rising edge




library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity SR_par2ser_redge is
  generic (
    width : integer := 16);


  port (
    clk      : in  std_logic;
    DataIn   : in  std_logic_vector(width-1 downto 0);
    load     : in  std_logic;
    shift_en : in  std_logic;
    reset    : in  std_logic;
    DataOut  : out std_logic);

end SR_par2ser_redge;

architecture SR_par2ser_arch of SR_par2ser_redge is

  signal data_int : std_logic_vector(width-1 downto 0);


begin

  SHIFT_REG: process (clk, reset)
  begin

    if reset = '1' then                 -- asynchronous reset
      data_int <= (others => '0');

    elsif rising_edge(clk) then
      if (load = '1') then
        data_int <= DataIn;

      elsif (shift_en = '1') then
        for i in width-2 downto 0 loop
          data_int(i+1) <= data_int(i);
        end loop;
      end if;

    end if;
  end process SHIFT_REG;

  DataOut <= data_int(width-1);
```

```
end SR_par2ser_arch;
```

Listing: Clock divider

```
-- Author       : Tore André Bekkeng
-- Company      : University of Oslo
-- File name    : clock18iv.vhd
-- Date         : 31.08.08
-- Version      : 02
-- Project      : ICI-2
-- Function     : Clock divider; divide with 18



library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;


entity clock18div is

  port
    (
    clk_in  : in  std_logic;
    reset   : in  std_logic;
    clk_out : out std_logic
    );

end clock18div;



architecture clock_div_arch of clock18div is


constant DivFactor : integer := 18;
constant DivFactor_half : integer := 9;



begin



-- Dividing the input clock with DivFactor
CLK_DIV:
process (clk_in, reset)

variable div_cnt : integer range 0 to DivFactor - 1;

begin

   if reset = '1' then                  -- asynchronous reset
     div_cnt := 0;
     clk_out<= '0';

   elsif rising_edge(clk_in) then
     if (div_cnt = DivFactor - 1) then
         div_cnt := 0;
     else
       div_cnt := div_cnt + 1;
     end if;
```

```
      if (div_cnt >= DivFactor_half) then
        clk_out <= '0';
      else
        clk_out <= '1';
      end if;

   end if;
end process CLK_DIV;


end clock_div_arch;
```

Listing: Component package (all not used)

```
-- Author        : Tore André Bekkeng
-- Company       : University of Oslo
-- File name     : comp_package.vhd
-- Date          :  24.03.08
-- Version       : 01
-- Project       : CFBLP - ICI 2
-- Package       : Components used for CFBLP on ICI-2



library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

package comp_package is

-------------------------------------------------------------------------------
--                          COMPONENT DECLARATIONS
-------------------------------------------------------------------------------

component SR_par2ser_fedge
    generic (
      width : integer);

    port
      (
      clk      : in  std_logic;
      DataIn   : in  std_logic_vector(width-1 downto 0);
      load     : in  std_logic;
      shift_en : in  std_logic;
      reset    : in  std_logic;
      DataOut  : out std_logic
      );
end component;

-------------------------------------------------------------------------------

component SR_par2ser_redge
    generic (
      width : integer);

    port
      (
      clk      : in  std_logic;
      DataIn   : in  std_logic_vector(width-1 downto 0);
      load     : in  std_logic;
      shift_en : in  std_logic;
      reset    : in  std_logic;
      DataOut  : out std_logic
      );
end component;


-------------------------------------------------------------------------------

component  SR_SerIn_redge
```

```
  generic (
    width : integer);

  port
    (
    clk      : in  std_logic;
    DataIn   : in  std_logic;
    shift_en : in  std_logic;
    DataOut  : out std_logic_vector(width-1 downto 0)
    );
end component;
```

```
component Sync_Counter

  generic (
    CounterSize : integer);

  port
    (
    clk    : in         std_logic;
    areset : in         std_logic;
    enable : in         std_logic;
    count  : buffer     std_logic_vector(CounterSize-1 downto 0)
    );

end component;
```

```
component Sync_Counter_fedge

  generic (
    CounterSize : integer);

  port
    (
    clk    : in         std_logic;
    areset : in         std_logic;
    enable : in         std_logic;
    count  : buffer     std_logic_vector(CounterSize-1 downto 0)
    );

end component;


-- 16 bit
component TwoComp2Binary

   port
    (
    twoComp : in  std_logic_vector(15 downto 0);
    bin     : out std_logic_vector(15 downto 0)
    );

end component;
```

```
end comp_package;
```